



MS_7623 VER:1.0

CPU:

AMD AM3

System Chipset:

AMD/ATI 740G/760G

AMD/ATI RS710

On Board Chipset:

FINTEK Super I/O -- F71889 F

LAN -- AR8132M/AR8131M

HD Codec -- ALC888S/889

BIOS -- SPI ROM 16M

Main Memory:

DDR III X 2 (Max 8GB)

Expansion Slots:

PCI-E X1 X2

PCI-E X16 X1

PCI 2.2 Slot X1

Clock Generator:

Controller--RTM-880N-793

PWM:

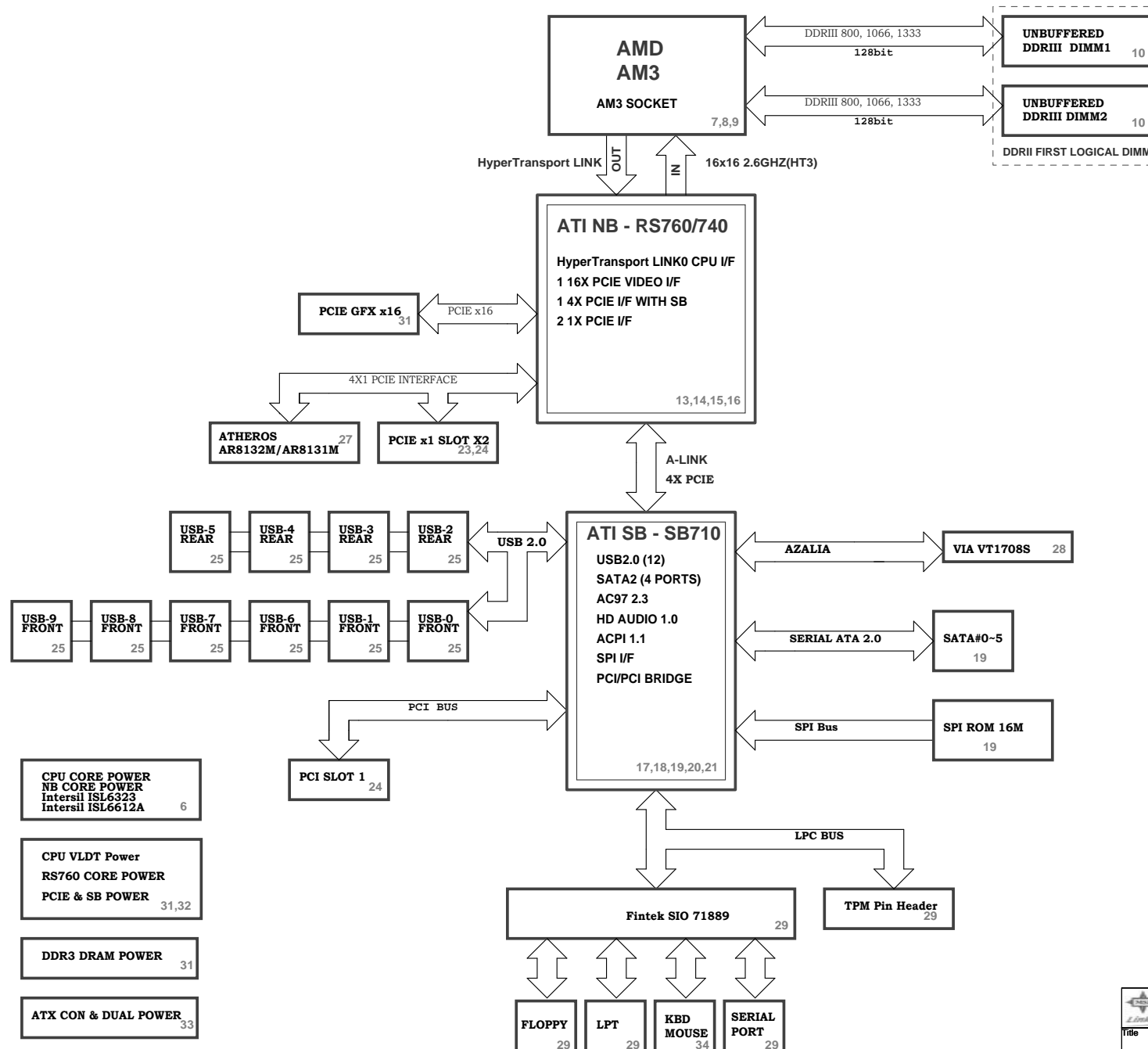
INTSIL6323A

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CFG_7623_4M3E: 740G + SB710, 10/100LAN, 3孔audio jack, ACC, all EL CAP
CFG_7623_4M3H: 740G + SB710, 10/100LAN, 3孔audio jack, ACC, 半固CAP
CFG_7623_4G6H: 740G + SB710, Gb LAN, 6孔audio jack, APS, OC-switch, ACC, 半固CAP
CFG_7623_6G6H: 760G + SB710, Gb LAN, 6孔audio jack, APS, OC-switch, ACC, 半固電容
CFG_7623_6G6S: 760G + SB710, Gb LAN, 6孔audio jack, APS, OC-switch, ACC, 全固
注: CFG_7623_ABCD, 这里ABCD分別代表:
A: (4) 740G; (6) 760G
B: (M) Mega Lan; (G) GIGA LAN
C: (3) Audio 3Hole; (6) Audio 6Hole
D: (E) EL Cap; (H) Half Solid Cap; (S) Colid Cap

Micro Star Restricted Secret		
Title	Cover Sheet	Rev
Document Number	MS_7623	1.0
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, September 28, 2009 Sheet 1 of 37

Project RS-740/760 BLOCK DIAGRAM

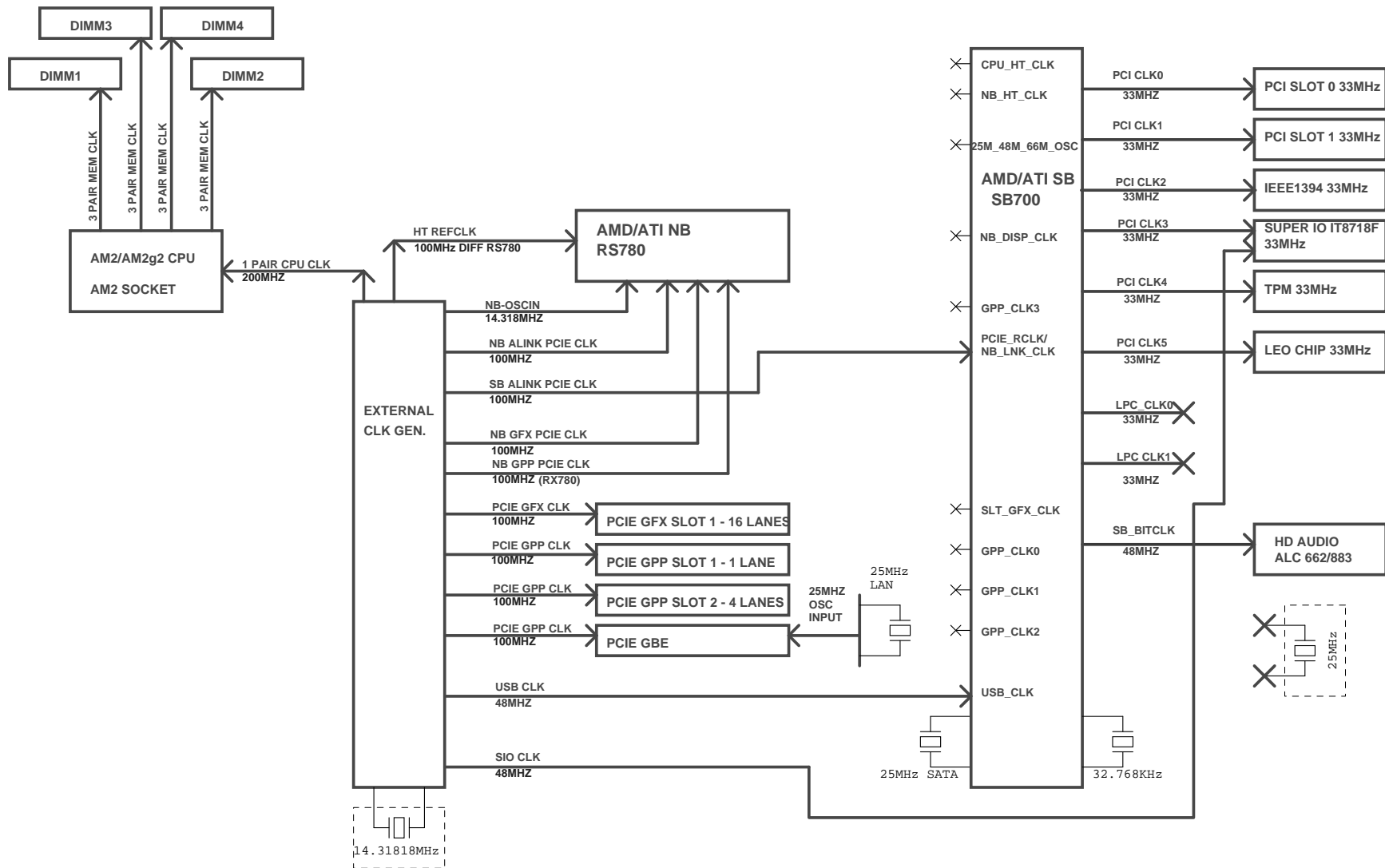


SB700/750 GPIO Config

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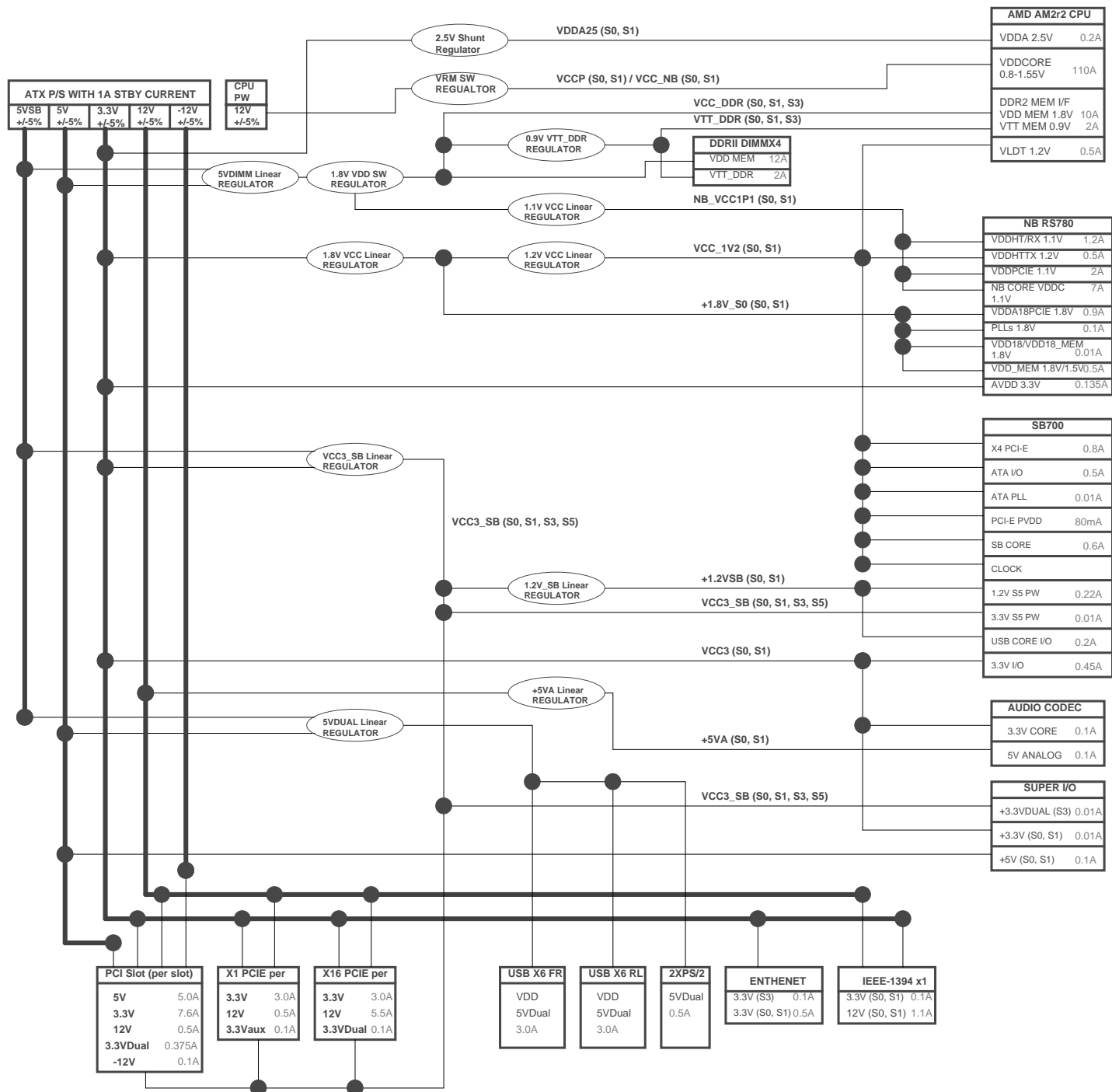
PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INTH# PCI_INTH# PCI_INTE#	PREQ#1 PGNT#1	AD22	PCICLK1



External clock mode
Internal clock mode

Power Deliver Chart



The schematic diagram illustrates the ISL6323CR KCT for Hybride, a power management IC. It includes several key sections:

- Input Section:** Features a +12VIN input with a 10K resistor (R91) and a 10K resistor (R92) connected to the VCC5 pin. The VCC5 pin is also connected to a 10K resistor (R93) and a 10K resistor (R94).
- DC-DC Converters:** The diagram shows two DC-DC converters. The first converter has an input of 12V and an output of 5V, using a 10K resistor (R91) and a 10K resistor (R92). The second converter has an input of 12V and an output of 3.3V, using a 10K resistor (R93) and a 10K resistor (R94).
- Output Drivers:** The output drivers are connected to the VCC5 pin and the VCC3 pin. The VCC5 pin is connected to a 10K resistor (R91) and a 10K resistor (R92). The VCC3 pin is connected to a 10K resistor (R93) and a 10K resistor (R94).
- Signal Section:** The signal section includes a 12V input with a 10K resistor (R91) and a 10K resistor (R92). The signal is connected to the VCC5 pin and the VCC3 pin.

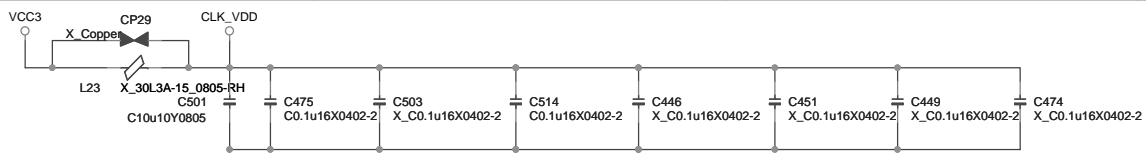
The diagram also includes a table of components and their values:

Component	Value
R91	10K
R92	10K
R93	10K
R94	10K

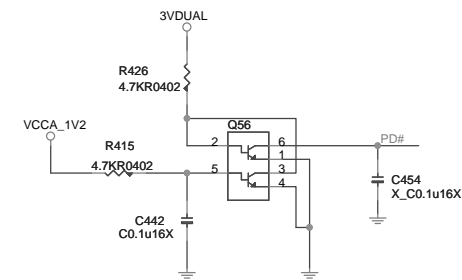
The diagram is labeled "ISL6323CR KCT for Hybride" and includes a note: "BOTTOM PAD CONNECT TO GND Through 8 VIAS".

L-MOS主料: D03-0603B2B-N03、AVL: D03-0480600-005,D03-004030B-N03

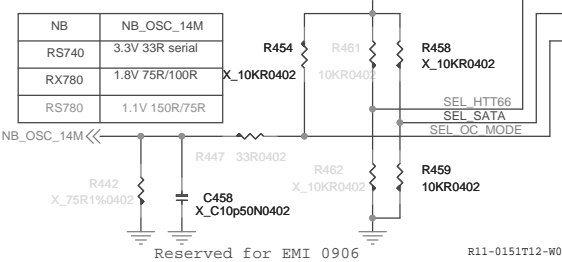
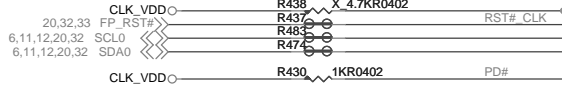
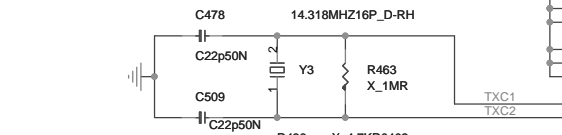
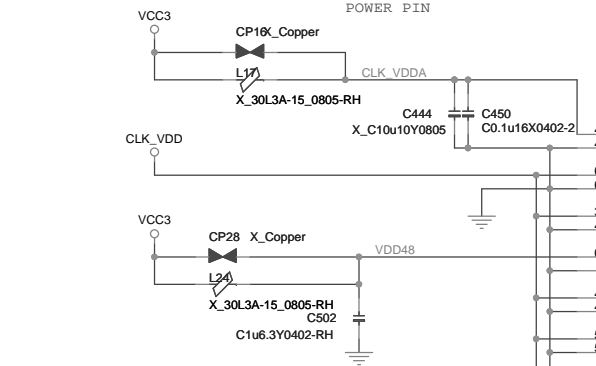
```
BUS_SEL=100%VCC
I2C address:0X60
R643=10K;R644=OPEN
```



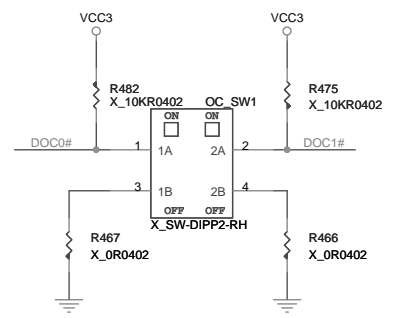
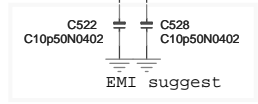
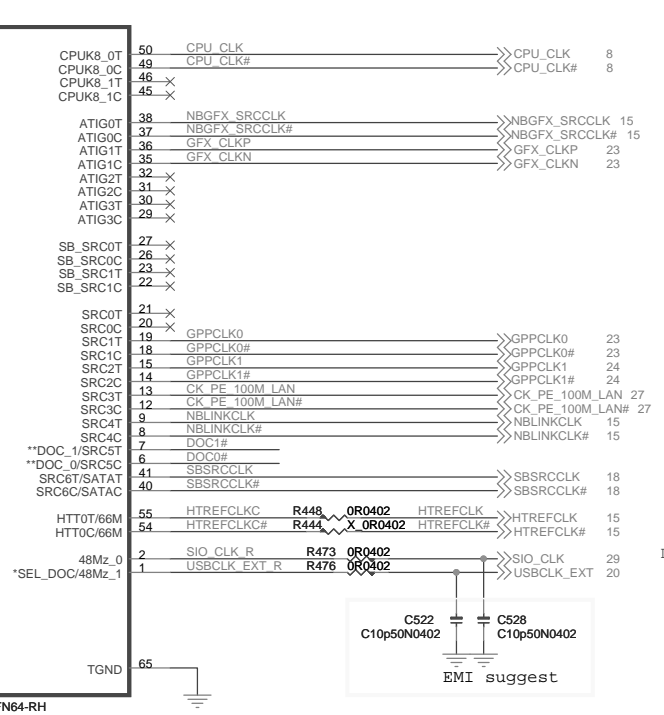
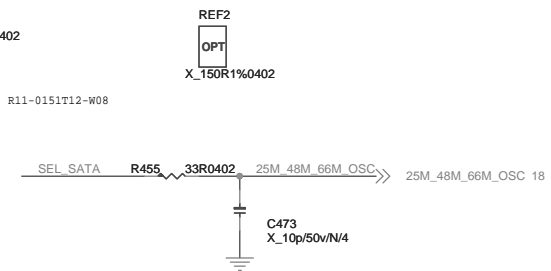
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U41 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U41 POWER PIN

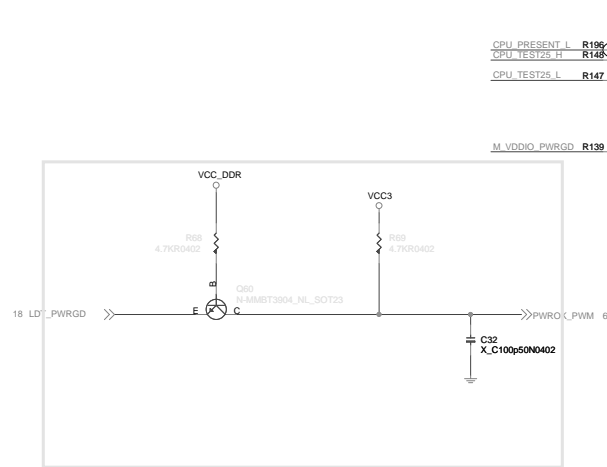
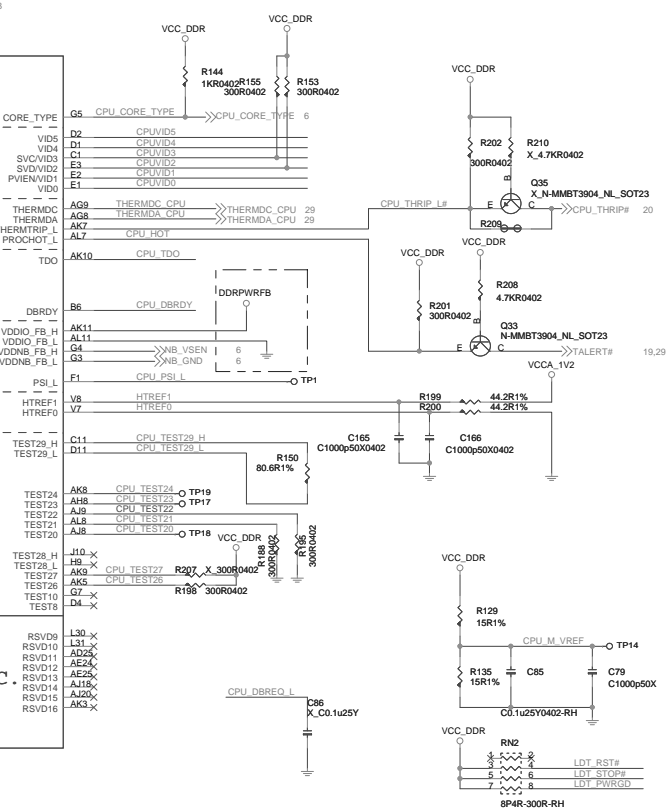
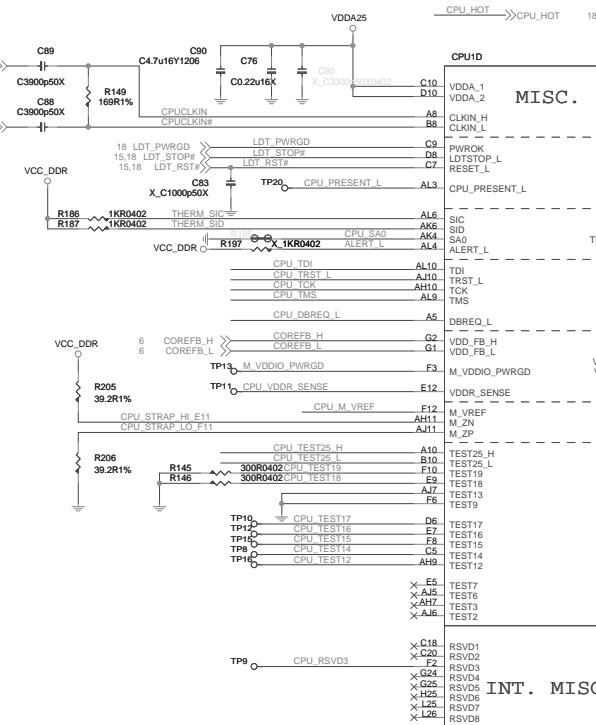
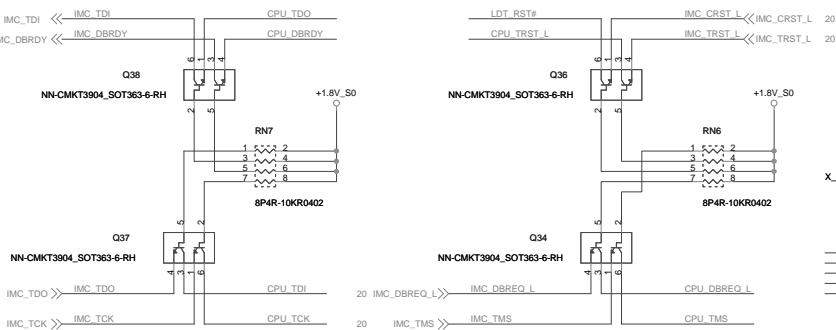


NN-CMKT3904_SOT363-RH



REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END





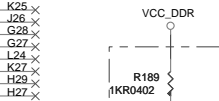
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11 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
11 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
11 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
11 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

CPU1B

11 MEM_MAO_CLK_H0 >> MEM_MAO_CLK_H0
11 MEM_MAO_CLK_L0 >> MEM_MAO_CLK_L0
11 MEM_MAO_CLK_H1 >> MEM_MAO_CLK_H1
11 MEM_MAO_CLK_L1 >> MEM_MAO_CLK_L1
11 MEM_MAO_CS_L1 >> MEM_MAO_CS_L1
11 MEM_MAO_CS_L0 >> MEM_MAO_CS_L0
11 MEM_MAO_ODT1 >> MEM_MAO_ODT1
11 MEM_MAO_ODT0 >> MEM_MAO_ODT0
11 MEM_MA_RESET# >> MEM_MA_RESET#
11 MEM_MA_CAS_L >> MEM_MA_CAS_L
11 MEM_MA_WE_L >> MEM_MA_WE_L
11 MEM_MA_RAS_L >> MEM_MA_RAS_L
11 MEM_MA_BANK2 >> MEM_MA_BANK2
11 MEM_MA_BANK1 >> MEM_MA_BANK1
11 MEM_MA_BANK0 >> MEM_MA_BANK0
11 MEM_MA_CKE1 >> MEM_MA_CKE1
11 MEM_MA_CKE0 >> MEM_MA_CKE0
11 MEM_MA_ADD15 >> MEM_MA_ADD15
11 MEM_MA_ADD14 >> MEM_MA_ADD14
11 MEM_MA_ADD13 >> MEM_MA_ADD13
11 MEM_MA_ADD12 >> MEM_MA_ADD12
11 MEM_MA_ADD11 >> MEM_MA_ADD11
11 MEM_MA_ADD10 >> MEM_MA_ADD10
11 MEM_MA_ADD9 >> MEM_MA_ADD9
11 MEM_MA_ADD8 >> MEM_MA_ADD8
11 MEM_MA_ADD7 >> MEM_MA_ADD7
11 MEM_MA_ADD6 >> MEM_MA_ADD6
11 MEM_MA_ADD5 >> MEM_MA_ADD5
11 MEM_MA_ADD4 >> MEM_MA_ADD4
11 MEM_MA_ADD3 >> MEM_MA_ADD3
11 MEM_MA_ADD2 >> MEM_MA_ADD2
11 MEM_MA_ADD1 >> MEM_MA_ADD1
11 MEM_MA_ADD0 >> MEM_MA_ADD0
11 MEM_MA_DQS_H7 >> MEM_MA_DQS_H7
11 MEM_MA_DQS_L7 >> MEM_MA_DQS_L7
11 MEM_MA_DQS_H6 >> MEM_MA_DQS_H6
11 MEM_MA_DQS_L6 >> MEM_MA_DQS_L6
11 MEM_MA_DQS_H5 >> MEM_MA_DQS_H5
11 MEM_MA_DQS_L5 >> MEM_MA_DQS_L5
11 MEM_MA_DQS_H4 >> MEM_MA_DQS_H4
11 MEM_MA_DQS_L4 >> MEM_MA_DQS_L4
11 MEM_MA_DQS_H3 >> MEM_MA_DQS_H3
11 MEM_MA_DQS_L3 >> MEM_MA_DQS_L3
11 MEM_MA_DQS_H2 >> MEM_MA_DQS_H2
11 MEM_MA_DQS_L2 >> MEM_MA_DQS_L2
11 MEM_MA_DQS_H1 >> MEM_MA_DQS_H1
11 MEM_MA_DQS_L1 >> MEM_MA_DQS_L1
11 MEM_MA_DQS_H0 >> MEM_MA_DQS_H0
11 MEM_MA_DQS_L0 >> MEM_MA_DQS_L0
11 MEM_MA_DM7 >> MEM_MA_DM7
11 MEM_MA_DM6 >> MEM_MA_DM6
11 MEM_MA_DM5 >> MEM_MA_DM5
11 MEM_MA_DM4 >> MEM_MA_DM4
11 MEM_MA_DM3 >> MEM_MA_DM3
11 MEM_MA_DM2 >> MEM_MA_DM2
11 MEM_MA_DM1 >> MEM_MA_DM1
11 MEM_MA_DM0 >> MEM_MA_DM0

MEM_CHA

MA_CLK_H7
MA_CLK_L7
MA_CLK_H6
MA_CLK_L6
MA_CLK_H5
MA_CLK_L5
MA_CLK_H4
MA_CLK_L4
MA_CLK_H3
MA_CLK_L3
MA_CLK_H2
MA_CLK_L2
MA_CLK_H1
MA_CLK_L1
MA_CLK_H0
MA_CLK_L0
MA_CS_L1
MA_CS_L0
MA_ODT1
MA_ODT0
MA1_CS_L1
MA1_CS_L0
MA1_ODT1
MA1_ODT0
MA_RESET_L
MA_CAS_L
MA_WE_L
MA_RAS_L
MA_BANK2
MA_BANK1
MA_BANK0
MA_CKE1
MA_CKE0
MA_ADD15
MA_ADD14
MA_ADD13
MA_ADD12
MA_ADD11
MA_ADD10
MA_ADD9
MA_ADD8
MA_ADD7
MA_ADD6
MA_ADD5
MA_ADD4
MA_ADD3
MA_ADD2
MA_ADD1
MA_ADD0
MA_DQS_H7
MA_DQS_L7
MA_DQS_H6
MA_DQS_L6
MA_DQS_H5
MA_DQS_L5
MA_DQS_H4
MA_DQS_L4
MA_DQS_H3
MA_DQS_L3
MA_DQS_H2
MA_DQS_L2
MA_DQS_H1
MA_DQS_L1
MA_DQS_H0
MA_DQS_L0
MA_DM7
MA_DM6
MA_DM5
MA_DM4
MA_DM3
MA_DM2
MA_DM1
MA_DM0
MA_EVENT_L



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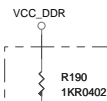
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12 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
12 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
12 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
12 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]

CPU1C

12 MEM_MB0_CLK_H0 >> MEM_MB0_CLK_H0
12 MEM_MB0_CLK_L0 >> MEM_MB0_CLK_L0
12 MEM_MB0_CLK_H1 >> MEM_MB0_CLK_H1
12 MEM_MB0_CLK_L1 >> MEM_MB0_CLK_L1
12 MEM_MB0_CS_L1 >> MEM_MB0_CS_L1
12 MEM_MB0_CS_L0 >> MEM_MB0_CS_L0
12 MEM_MB0_ODT1 >> MEM_MB0_ODT1
12 MEM_MB0_ODT0 >> MEM_MB0_ODT0
12 MEM_MB_RESET# >> MEM_MB_RESET#
12 MEM_MB_CAS_L >> MEM_MB_CAS_L
12 MEM_MB_WE_L >> MEM_MB_WE_L
12 MEM_MB_RAS_L >> MEM_MB_RAS_L
12 MEM_MB_BANK2 >> MEM_MB_BANK2
12 MEM_MB_BANK1 >> MEM_MB_BANK1
12 MEM_MB_BANK0 >> MEM_MB_BANK0
12 MEM_MB_CKE1 >> MEM_MB_CKE1
12 MEM_MB_CKE0 >> MEM_MB_CKE0
12 MEM_MB_ADD15 >> MEM_MB_ADD15
12 MEM_MB_ADD14 >> MEM_MB_ADD14
12 MEM_MB_ADD13 >> MEM_MB_ADD13
12 MEM_MB_ADD12 >> MEM_MB_ADD12
12 MEM_MB_ADD11 >> MEM_MB_ADD11
12 MEM_MB_ADD10 >> MEM_MB_ADD10
12 MEM_MB_ADD9 >> MEM_MB_ADD9
12 MEM_MB_ADD8 >> MEM_MB_ADD8
12 MEM_MB_ADD7 >> MEM_MB_ADD7
12 MEM_MB_ADD6 >> MEM_MB_ADD6
12 MEM_MB_ADD5 >> MEM_MB_ADD5
12 MEM_MB_ADD4 >> MEM_MB_ADD4
12 MEM_MB_ADD3 >> MEM_MB_ADD3
12 MEM_MB_ADD2 >> MEM_MB_ADD2
12 MEM_MB_ADD1 >> MEM_MB_ADD1
12 MEM_MB_ADD0 >> MEM_MB_ADD0
12 MEM_MB_DQS_H7 >> MEM_MB_DQS_H7
12 MEM_MB_DQS_L7 >> MEM_MB_DQS_L7
12 MEM_MB_DQS_H6 >> MEM_MB_DQS_H6
12 MEM_MB_DQS_L6 >> MEM_MB_DQS_L6
12 MEM_MB_DQS_H5 >> MEM_MB_DQS_H5
12 MEM_MB_DQS_L5 >> MEM_MB_DQS_L5
12 MEM_MB_DQS_H4 >> MEM_MB_DQS_H4
12 MEM_MB_DQS_L4 >> MEM_MB_DQS_L4
12 MEM_MB_DQS_H3 >> MEM_MB_DQS_H3
12 MEM_MB_DQS_L3 >> MEM_MB_DQS_L3
12 MEM_MB_DQS_H2 >> MEM_MB_DQS_H2
12 MEM_MB_DQS_L2 >> MEM_MB_DQS_L2
12 MEM_MB_DQS_H1 >> MEM_MB_DQS_H1
12 MEM_MB_DQS_L1 >> MEM_MB_DQS_L1
12 MEM_MB_DQS_H0 >> MEM_MB_DQS_H0
12 MEM_MB_DQS_L0 >> MEM_MB_DQS_L0
12 MEM_MB_DM7 >> MEM_MB_DM7
12 MEM_MB_DM6 >> MEM_MB_DM6
12 MEM_MB_DM5 >> MEM_MB_DM5
12 MEM_MB_DM4 >> MEM_MB_DM4
12 MEM_MB_DM3 >> MEM_MB_DM3
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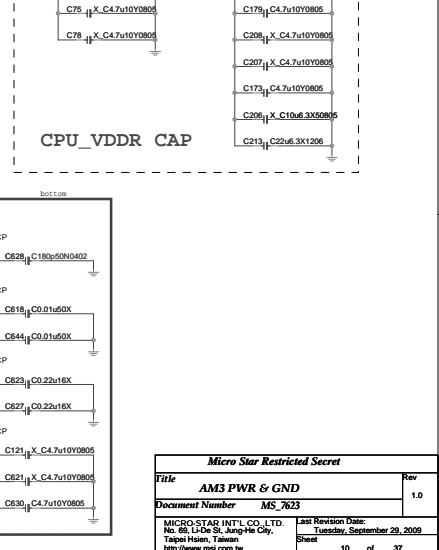
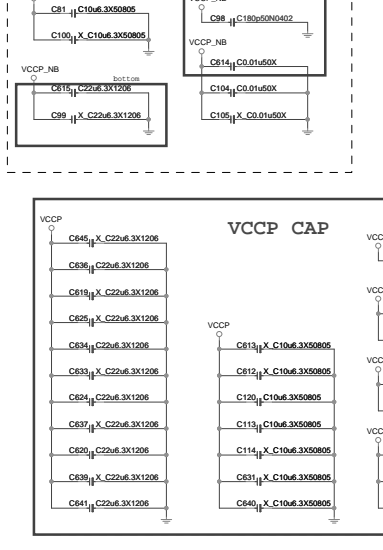
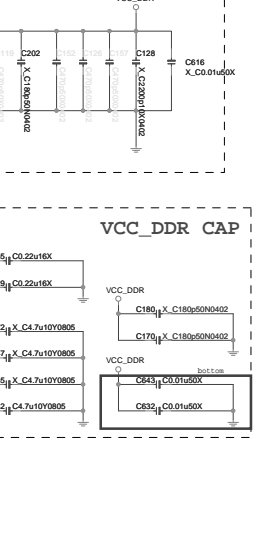
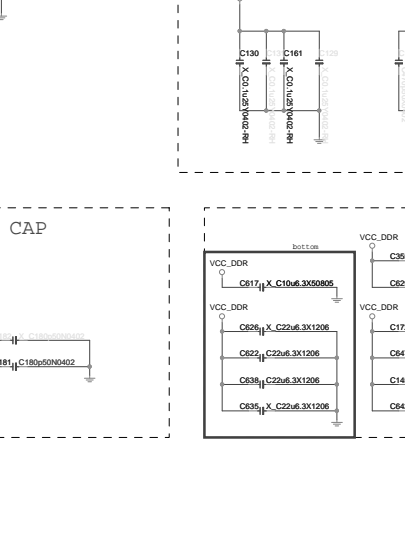
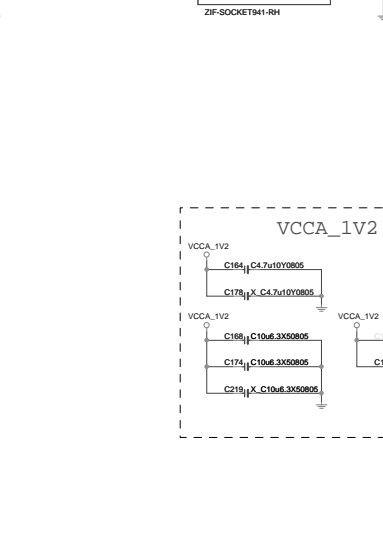
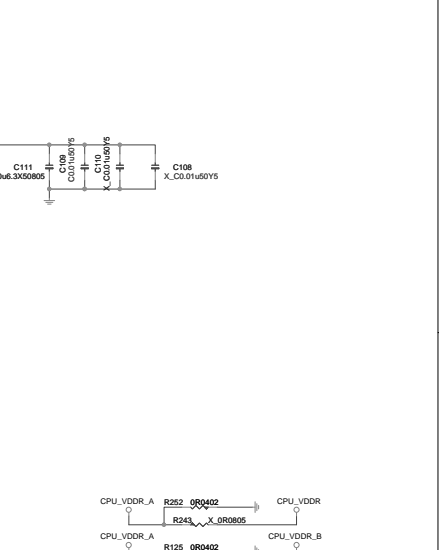
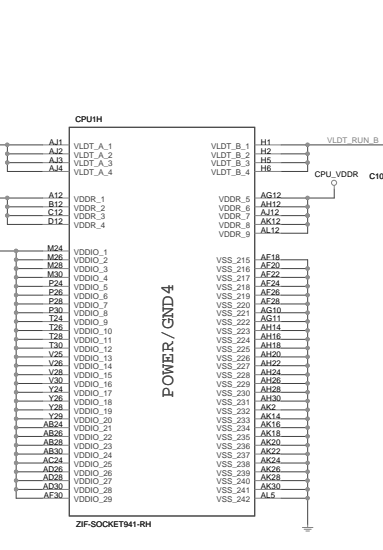
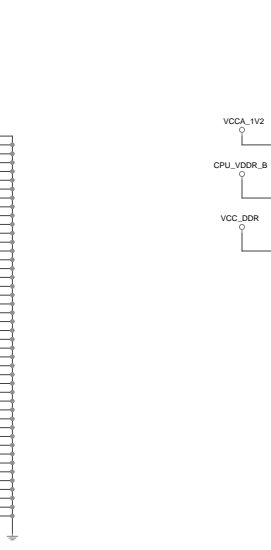
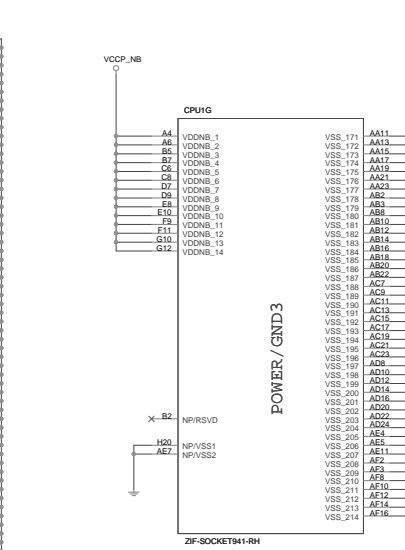
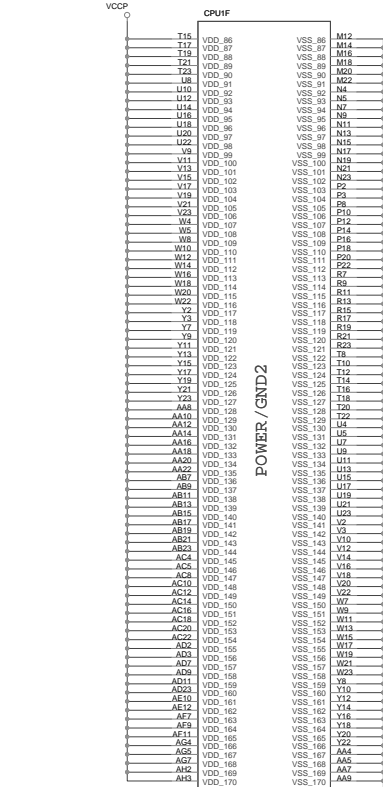
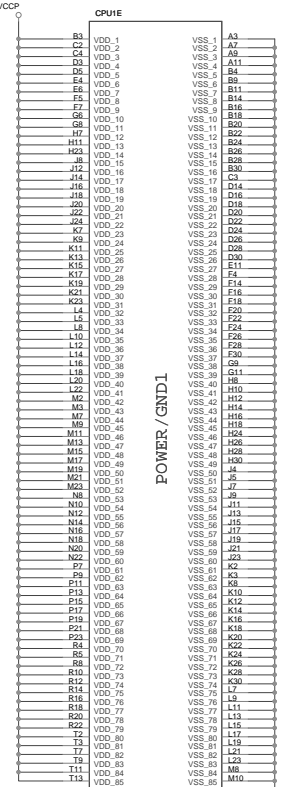
MEM_CHB

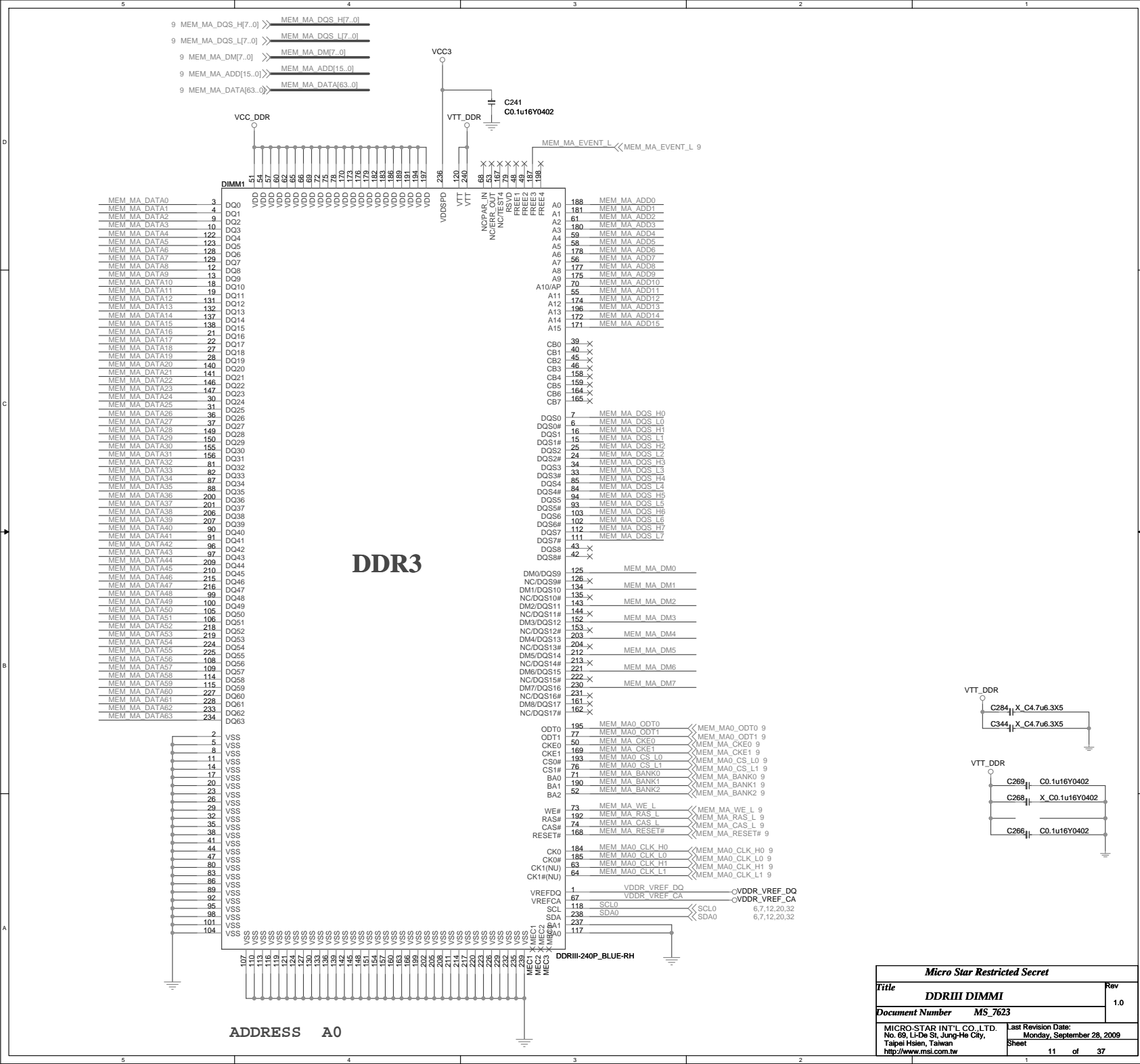
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MB_CLK_L5
MB_CLK_H4
MB_CLK_L4
MB_CLK_H3
MB_CLK_L3
MB_CLK_H2
MB_CLK_L2
MB_CLK_H1
MB_CLK_L1
MB_CLK_H0
MB_CLK_L0
MB_CS_L1
MB_CS_L0
MB_ODT1
MB_ODT0
MB1_CS_L1
MB1_CS_L0
MB1_ODT1
MB1_ODT0
MB_RESET_L
MB_CAS_L
MB_WE_L
MB_RAS_L
MB_BANK2
MB_BANK1
MB_BANK0
MB_CKE1
MB_CKE0
MB_ADD15
MB_ADD14
MB_ADD13
MB_ADD12
MB_ADD11
MB_ADD10
MB_ADD9
MB_ADD8
MB_ADD7
MB_ADD6
MB_ADD5
MB_ADD4
MB_ADD3
MB_ADD2
MB_ADD1
MB_ADD0
MB_DQS_H7
MB_DQS_L7
MB_DQS_H6
MB_DQS_L6
MB_DQS_H5
MB_DQS_L5
MB_DQS_H4
MB_DQS_L4
MB_DQS_H3
MB_DQS_L3
MB_DQS_H2
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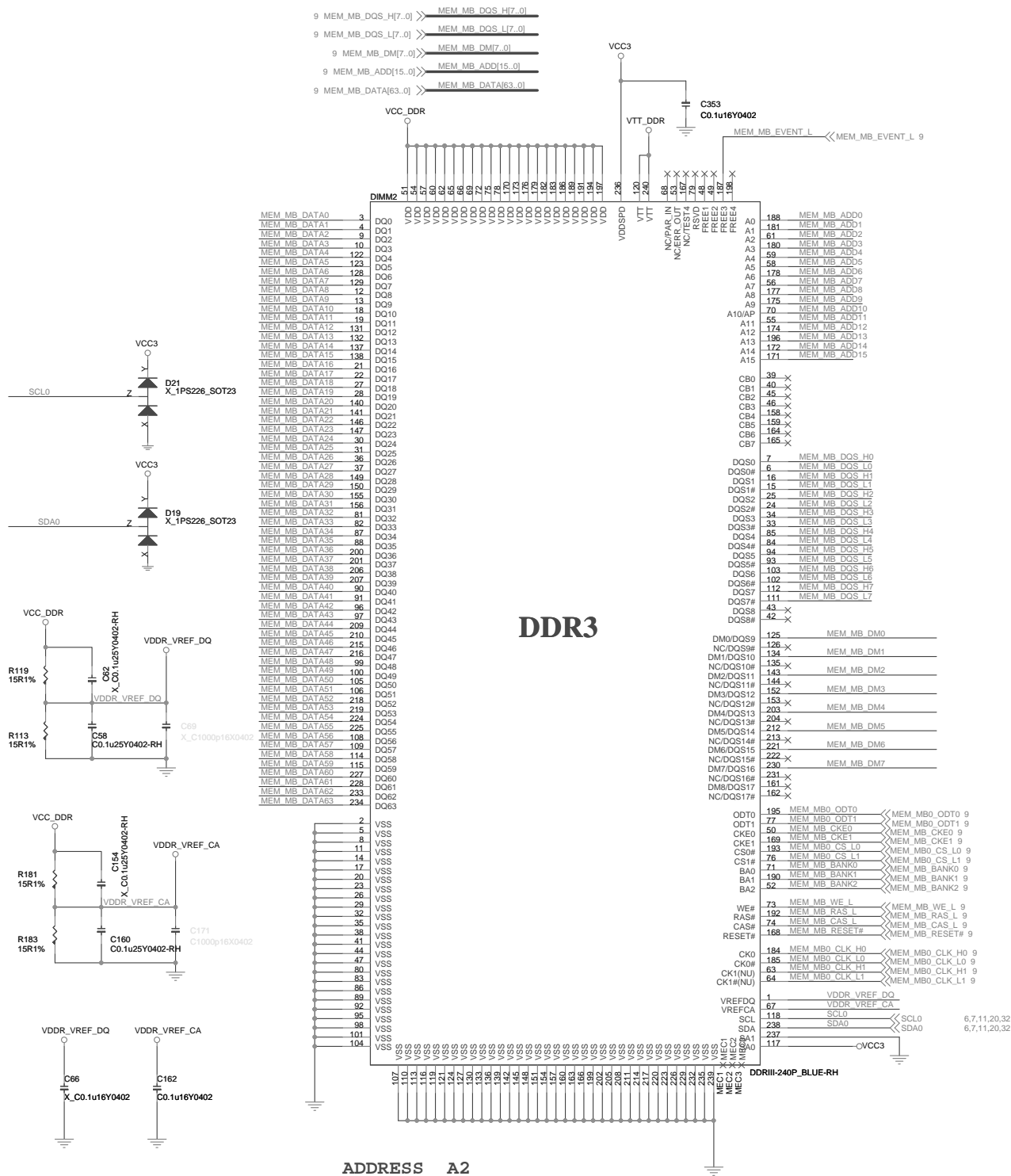


ZIF-SOCKET941-RH

Micro Star Restricted Secret	
Title	Rev
AM3 DDR MEMORY I/F	
Document Number	MS_7623
MICRO-STAR INT'L CO. LTD.	
No. 69, Li-Jie St., Jung-He City,	
Taipei Hsien, Taiwan	
http://www.msi.com.tw	
Last Revision Date:	
Monday, September 28, 2009	
Sheet	
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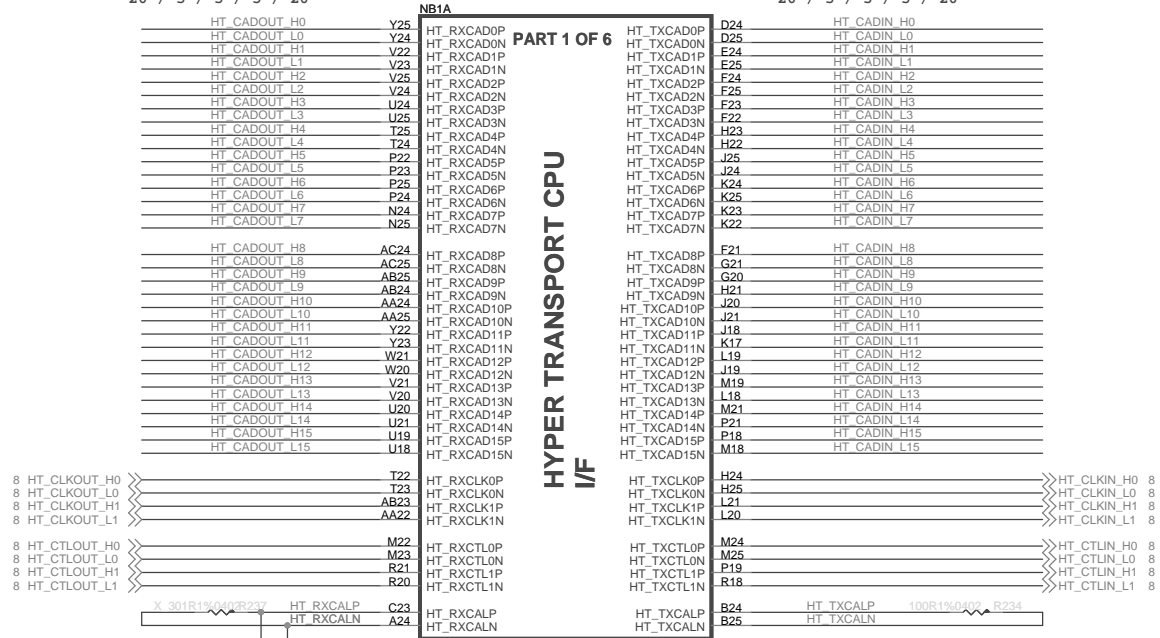


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8 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

8 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
8 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]

20 / 5 / 5 / 5 / 20

20 / 5 / 5 / 5 / 20



REF0

NB

X_760G

Check U10 New Version : Port Number

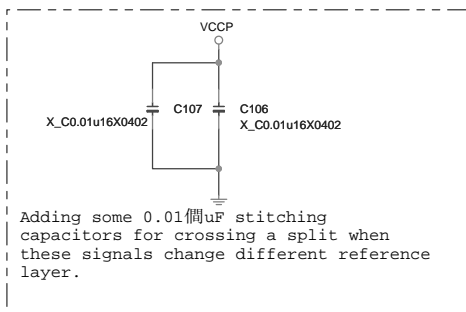
RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)	1.21K	301R
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			

REF1

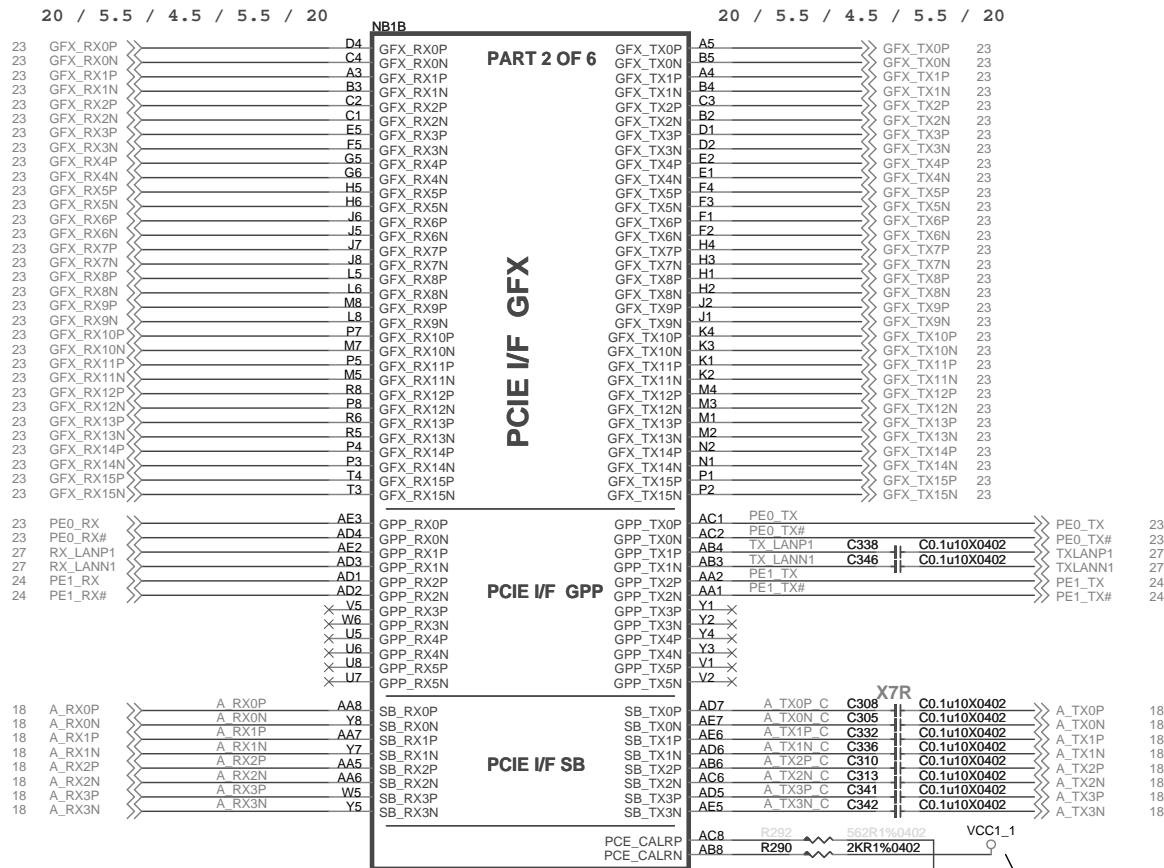
OPT

X_301R1%0402



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740G&760G-HT			
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AMD-215-0674007-00-A01-RH

RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

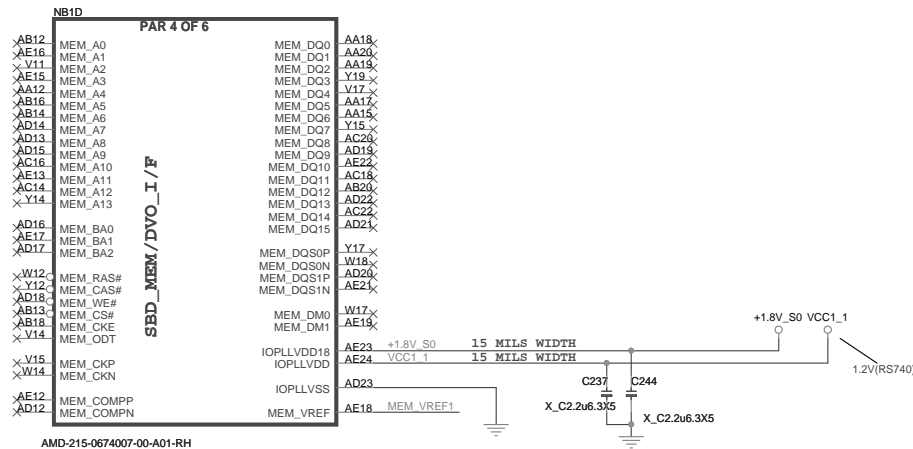
RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

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FOR RS780,R148,R162,C203 and C202 will be populated.

AMD: Please let MEM_VREF short to GND when Sideport is not used.

RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

15 RS740_DFT_GPIO1 >> R237 150R0402

15,26 VSYNC# >> R273 3KR0402
15 RS740_DFT_GPIO5 >> R282 X 3KR0402
15 RS740_DFT_GPIO5 >> R291 X 3KR0402

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

15 RS740_DFT_GPIO0 >> R307 X 3KR0402
15,26 HSYNC# >> R278 X 3KR0402
Have not side port memory,AMD suggest HSYNC pull high

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EEPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740: pin DFT_GPIO1

RS780: pin SUS_STAT#

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO

1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5

RS780: pin VSYNC

Enables Side port memory

1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)

RS740: pin DFT_GPIO0
RS780: pin HSYNC

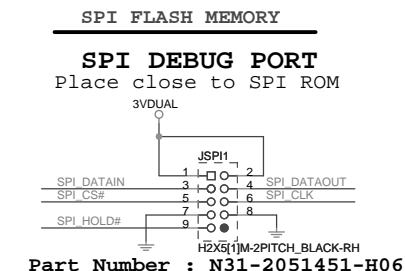
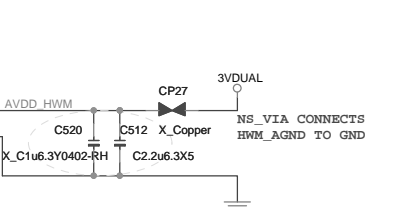
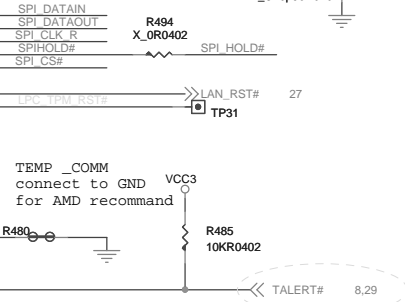
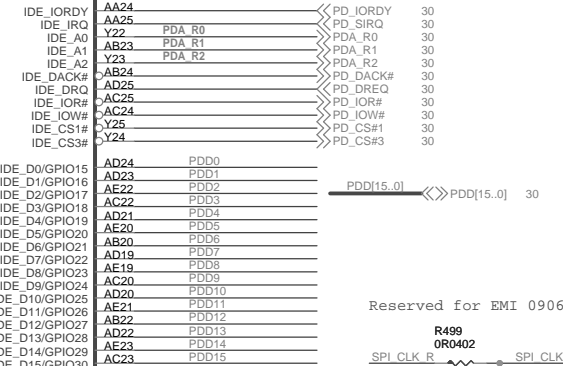
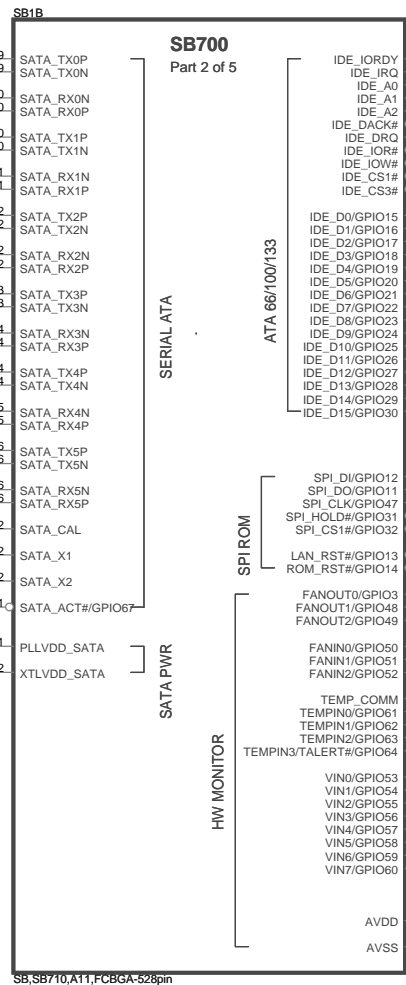
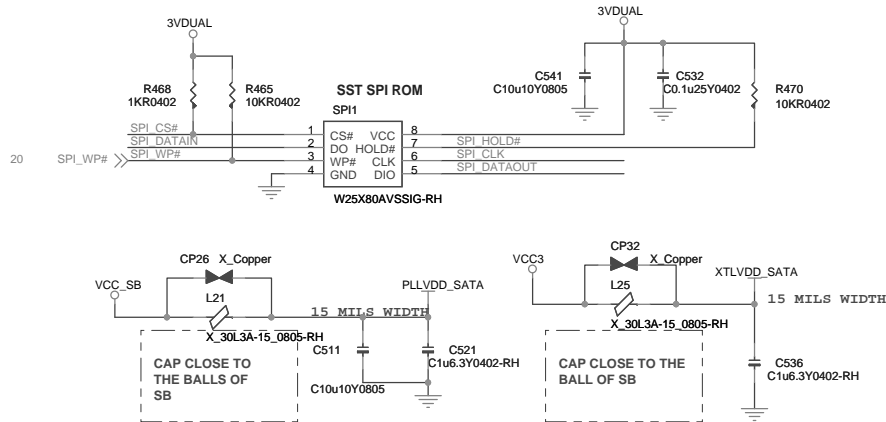
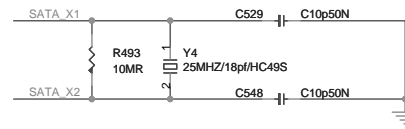
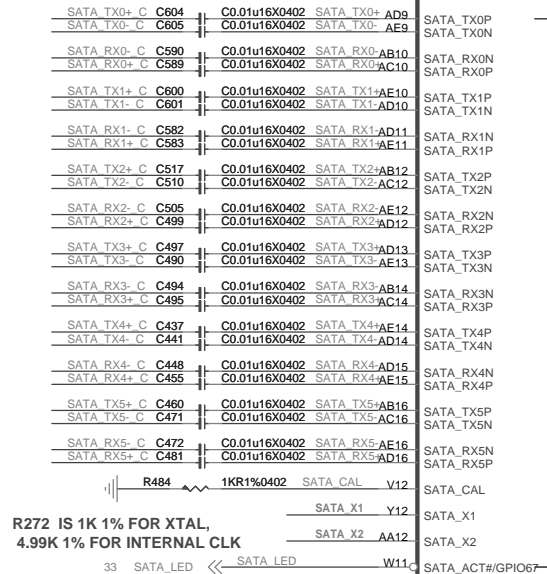
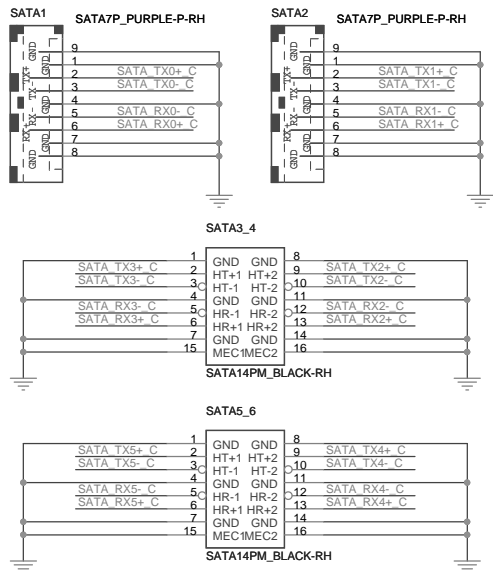
Enables Test debug bus using PCIE bus

1. Disable (can be enabled thru nbcfg register)
0 : Enable

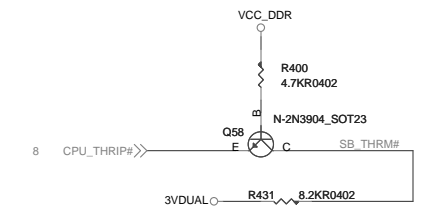
RS780: configurable thru register setting only
RS740: Not supported

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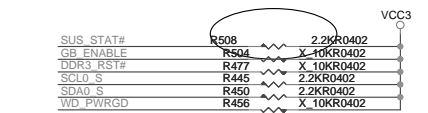
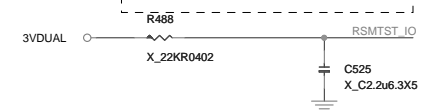
Title			
740G&760G-SPMEM/STRAPS			
Size	Document Number	Rev	
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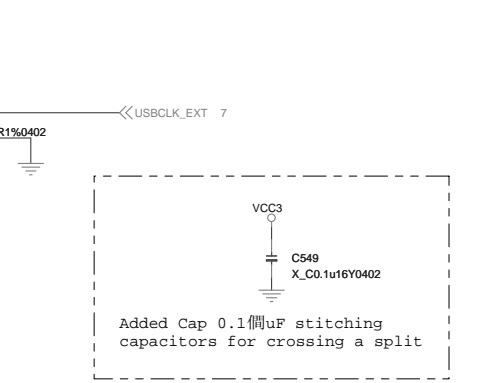
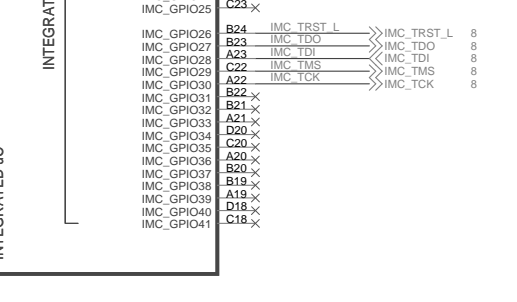
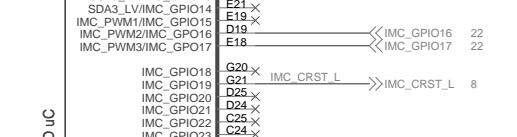
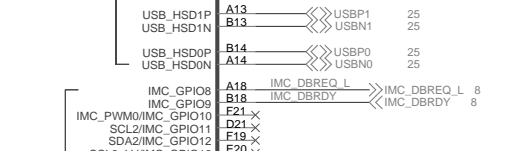
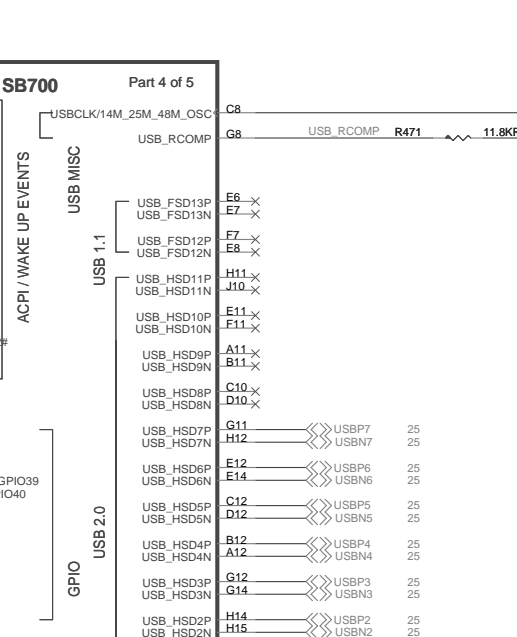
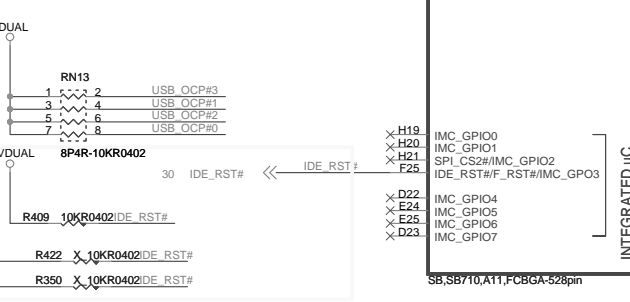
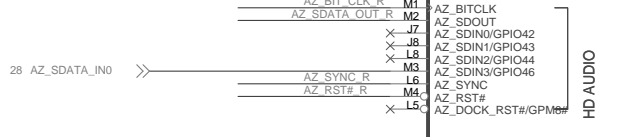
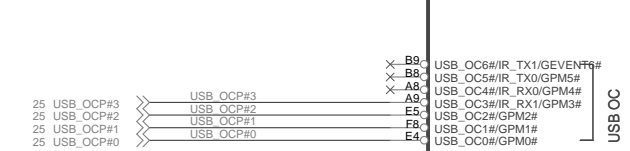
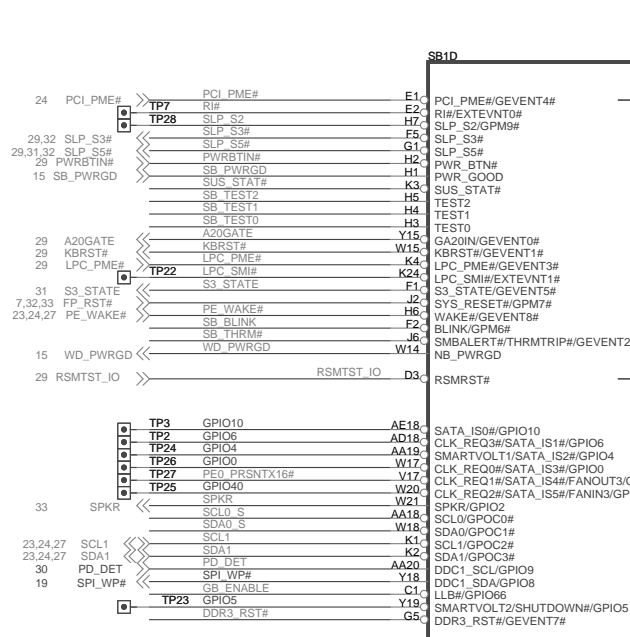
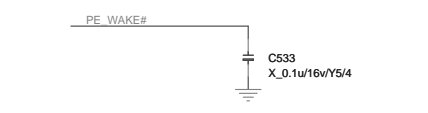
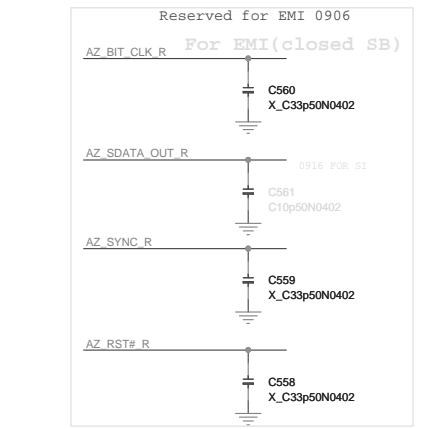
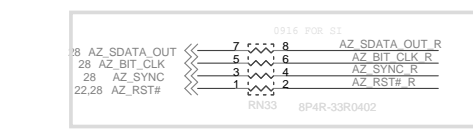
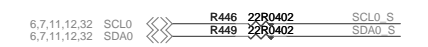
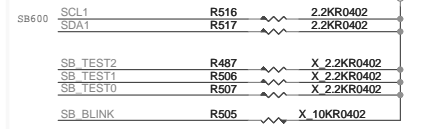
MICRO-STAR INT'L CO., LTD.			
Title	SB700-SATA/IDE/HWM/SPI		
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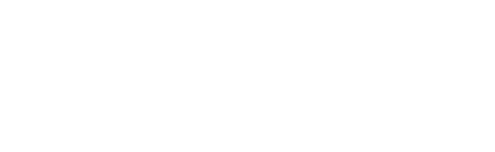
Cap have been unpopulate
for meet power sequence

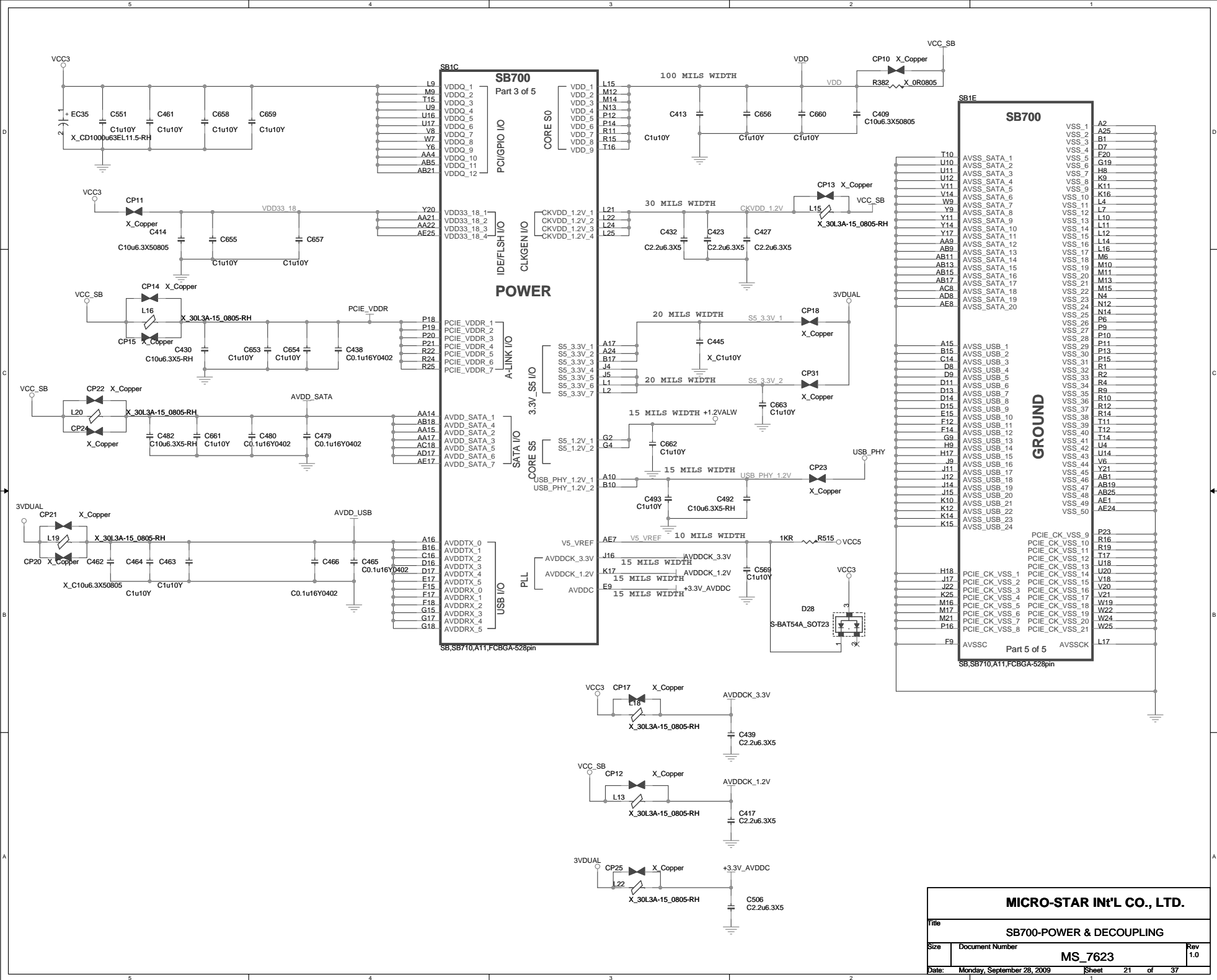


Pulling up to VCC3 change to 3VDUAL .Refer to AMD demo circuit



Added Cap 0.1uF stitching
capacitors for crossing a split

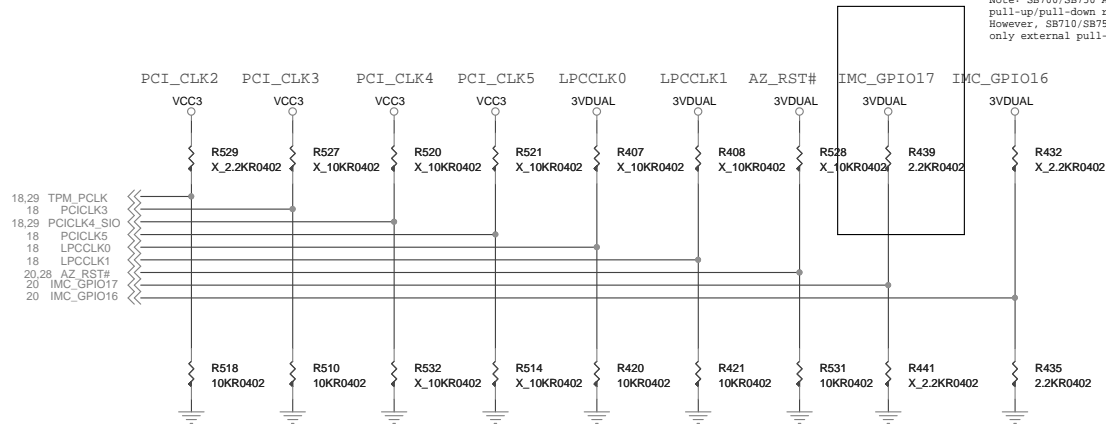






REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

DEBUG STRAPS

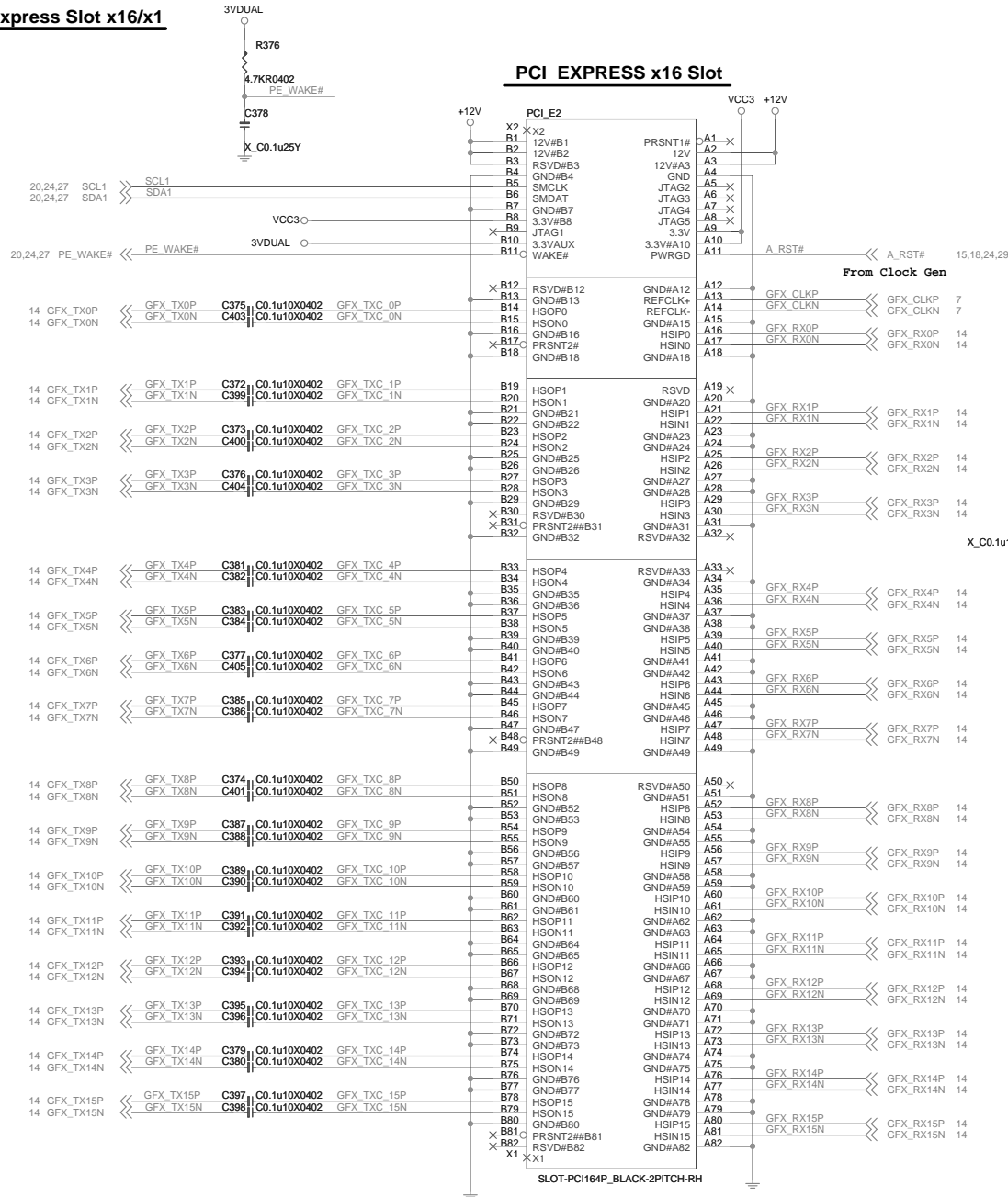
SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

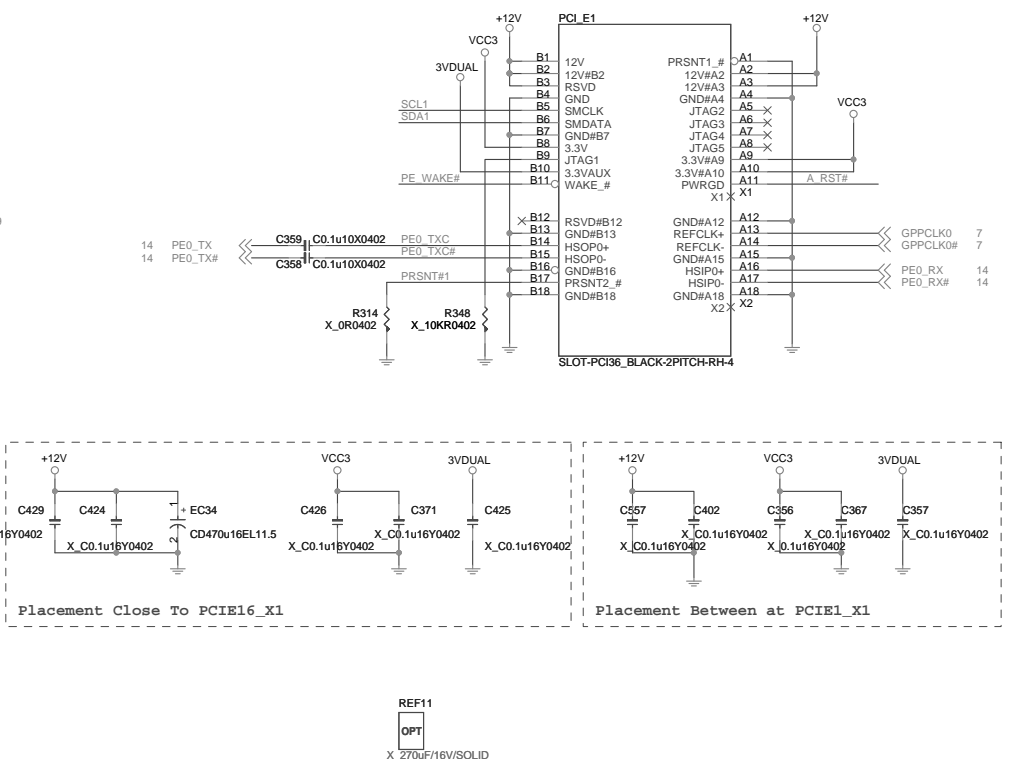
MICRO-STAR INT'L CO., LTD.

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SB700-STRAPS			
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PCI Express Slot x16/x1



PCI EXPRESS 1 Slot-1





Trace lengths must be less 12 inches

Trace lengths must be less 12 inches

20 USBP5 5
20 USBN5 6
20 USBP4 7
20 USBN4 8

L10

1 USBP5
2 USBN5
3 USBP4
4 USBN4

X_CMC-L12-181D017-LF

Match pairs to 50 mil.

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

USB LAN

5 USBP5
6 USBN5
7 USBP4
8 USBN4

LAN USB1A

1 USBP5
2 USBN5
3 USBP4
4 USBN4

RJ45_USB2_LEDx2_TX-100-RH-7

23
24
25
26
27
28
29
30

USB LAN

6 USBP5
4 USBP4
1 USBN5
3 USBN4

D16

ESD-IP4220

Figure 1: USB connector pin assignment. The figure contains three diagrams. The left diagram shows the pin assignment for a USB connector with pins 1 through 8, labeled USBP0, USBN0, USBP1, and USBN1. The middle diagram shows the pin assignment for a USB connector with pins 1 through 10, labeled USBP0, USBN0, USBP1, and USBN1. The right diagram shows the pin assignment for a USB connector with pins 1 through 6, labeled USBP0, USBN0, USBP1, and USBN1. The diagrams are labeled L26, X_CMC-L12-181D017-LF, H2X59M BLACK-RH, N31-2051581-H06, and ESD-IP4220.

[illegible]

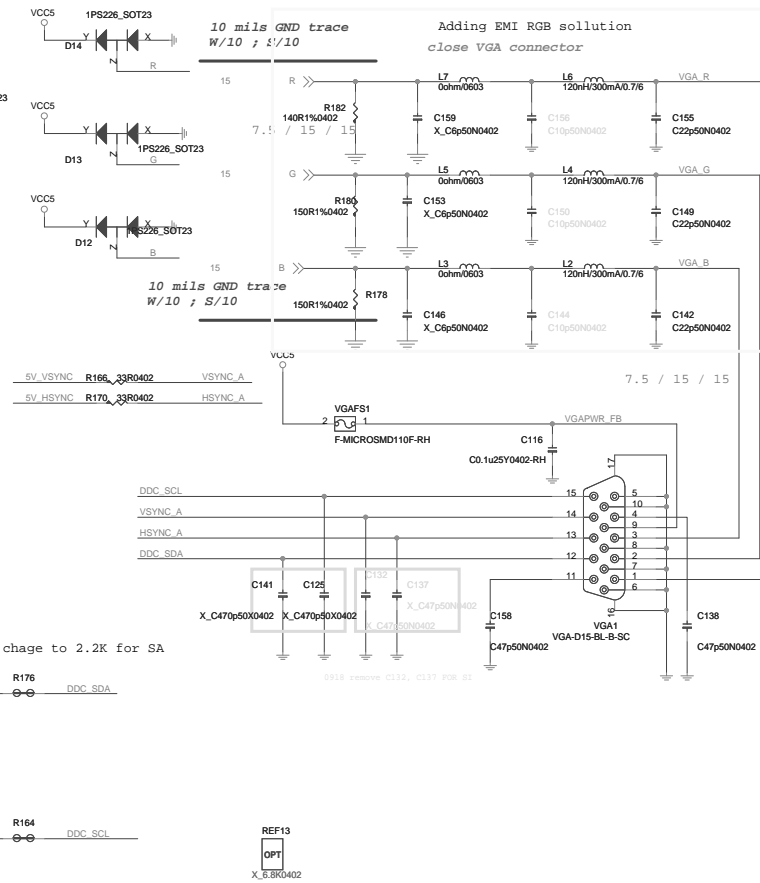
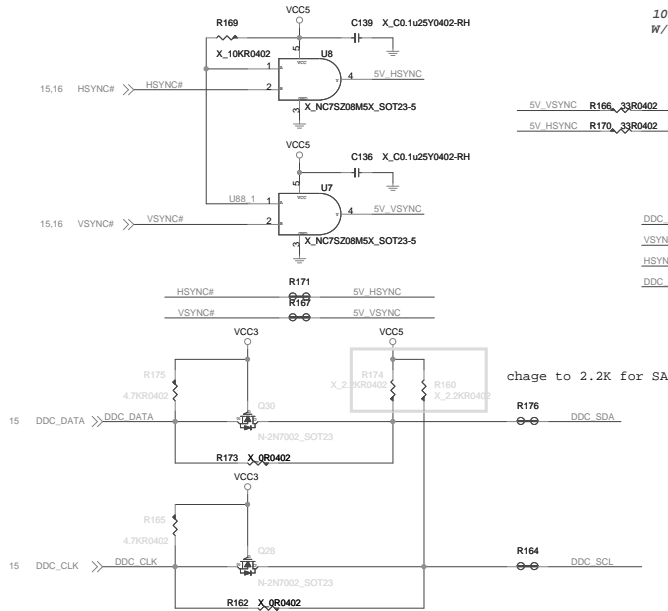
Trace lengths must be less 5 inches

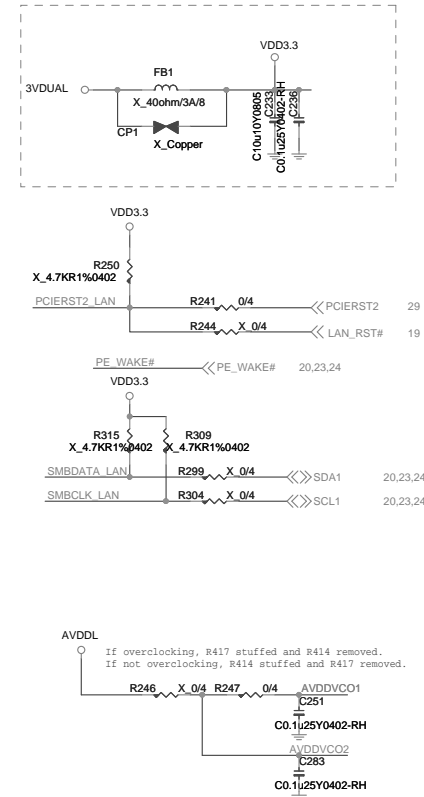
Match pairs to 50 mil.

NEAR USB CONNECTOR

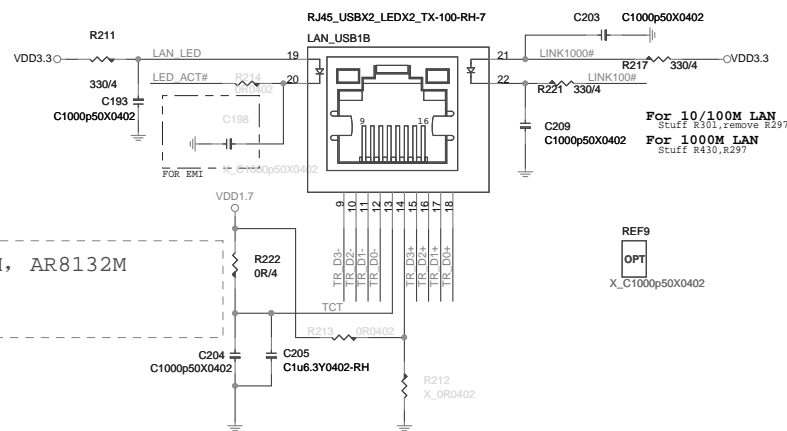
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

Figure 10 shows four circuit diagrams for connecting the X pin of the 1PS226_S0T23 MOSFET to VCC5. Each diagram consists of a MOSFET with its gate connected to a specific D pin (D8, D11, D10, or D9) and its source connected to pin N. The drain is connected to a specific output signal (DDC_SCL, DDC_SDA, HSYNC_A, or VSYNC_A). The X pin is connected to VCC5 through a resistor (D8, D11, D10, or D9).

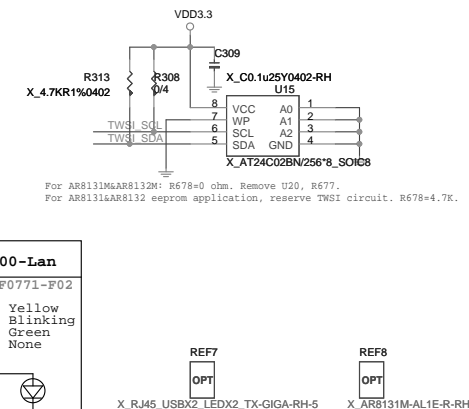
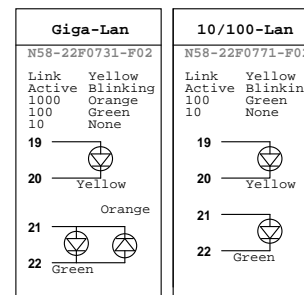




VDD3.3 power trace should be wider than 40mils
AVDDH power trace should be wider than 20mils
Pin1 to 4.7uH power trace should be wider than
60mils.
AVDDL, DVDDL and VDD1.7 power trace should be
wider than 20mils.

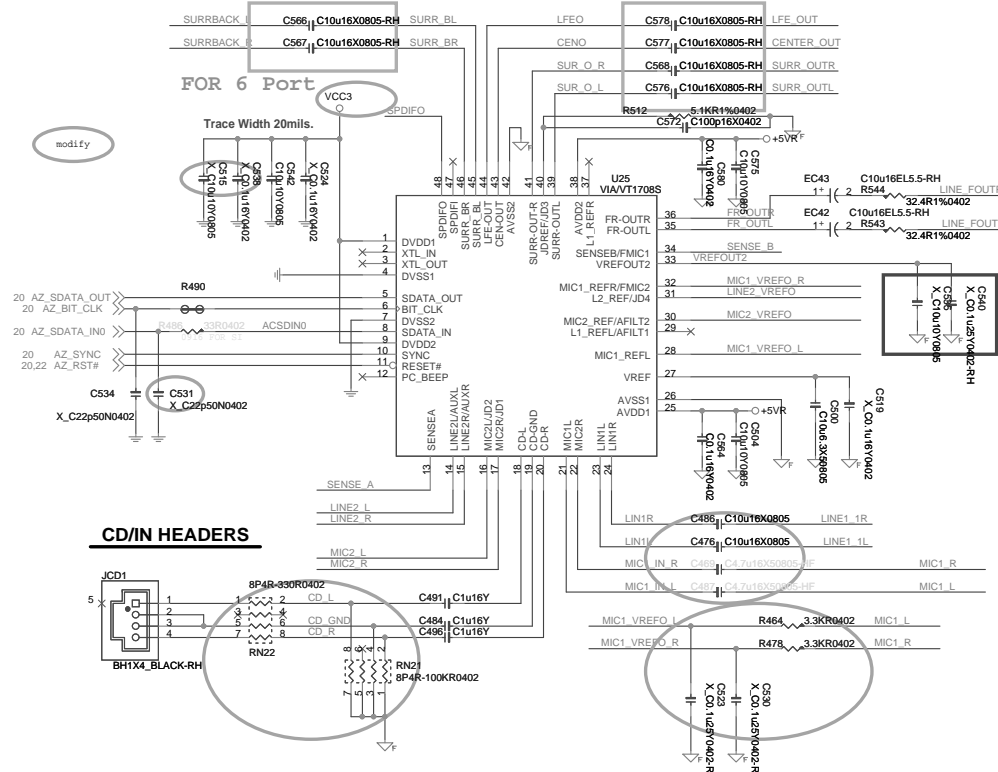


Note: AR8131M, AR8132M
R222必需上件

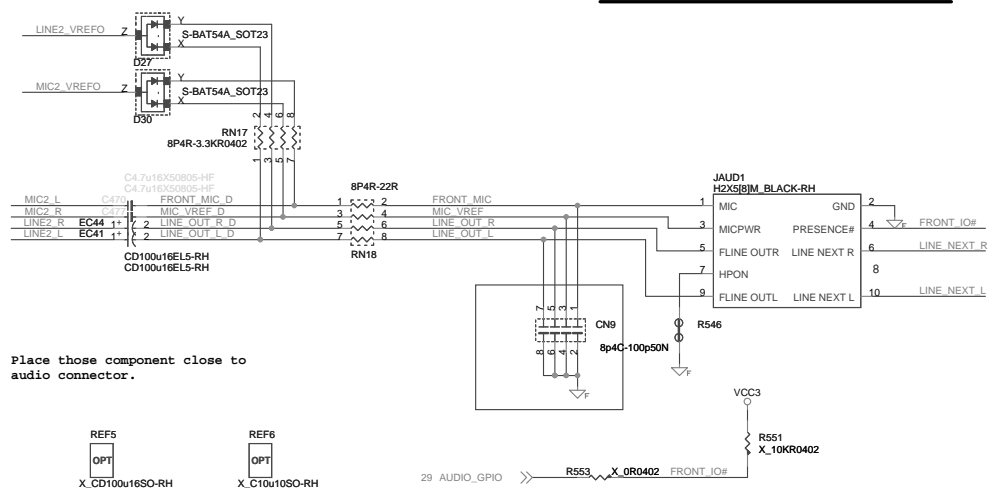


VT1708S CODEC

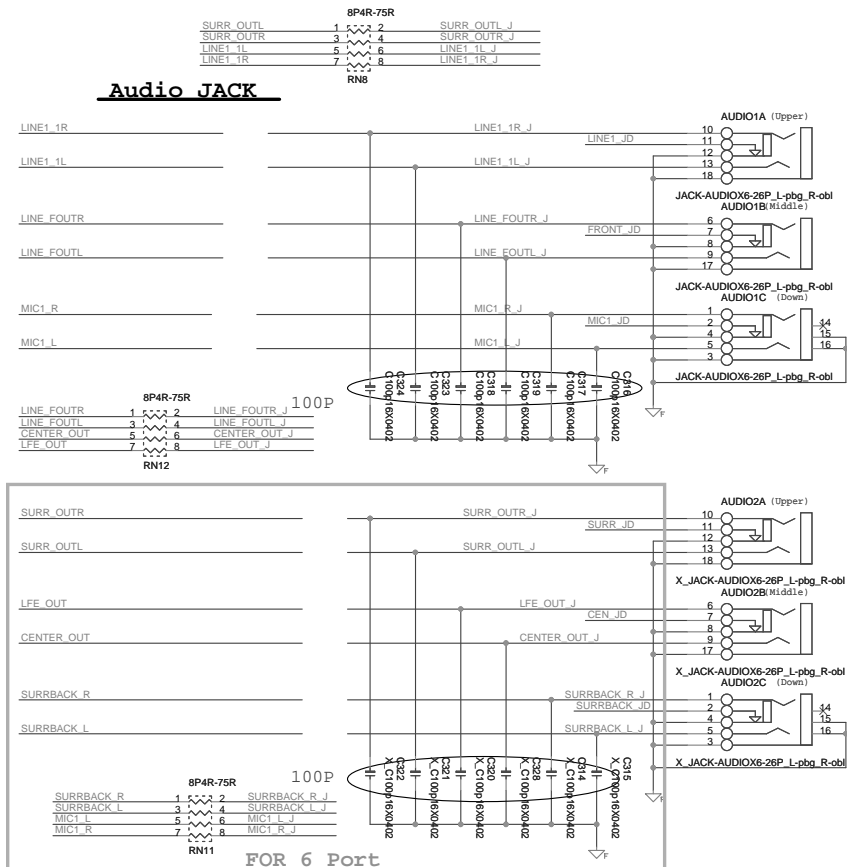
FOR 6 Port



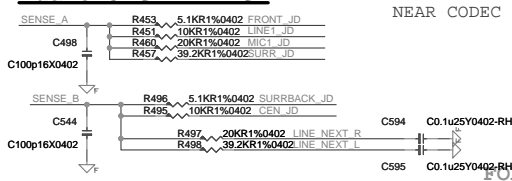
Azalia Front Audio Connector



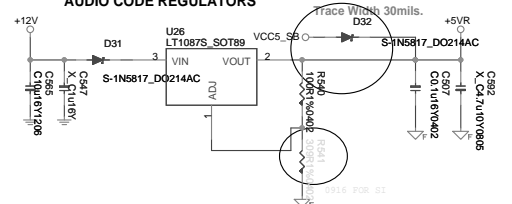
Audio JACK



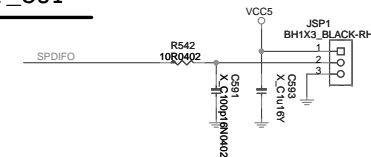
Audio JACK DETECT



AUDIO CODE REGULATORS



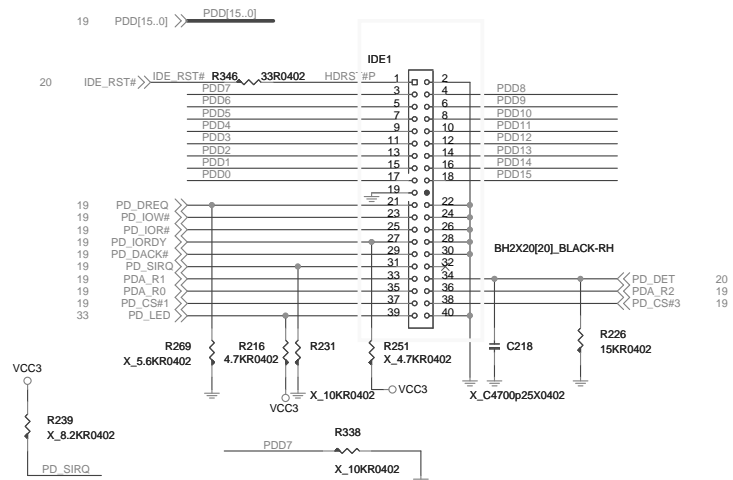
SPDIF OUT



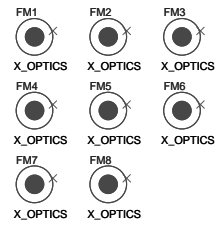
For EMI

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Title		VT1708S	
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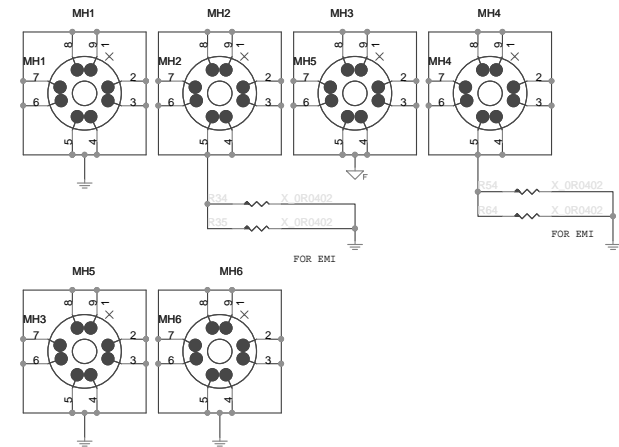
IDE 1



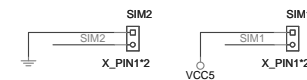
Optics Orientation Holes



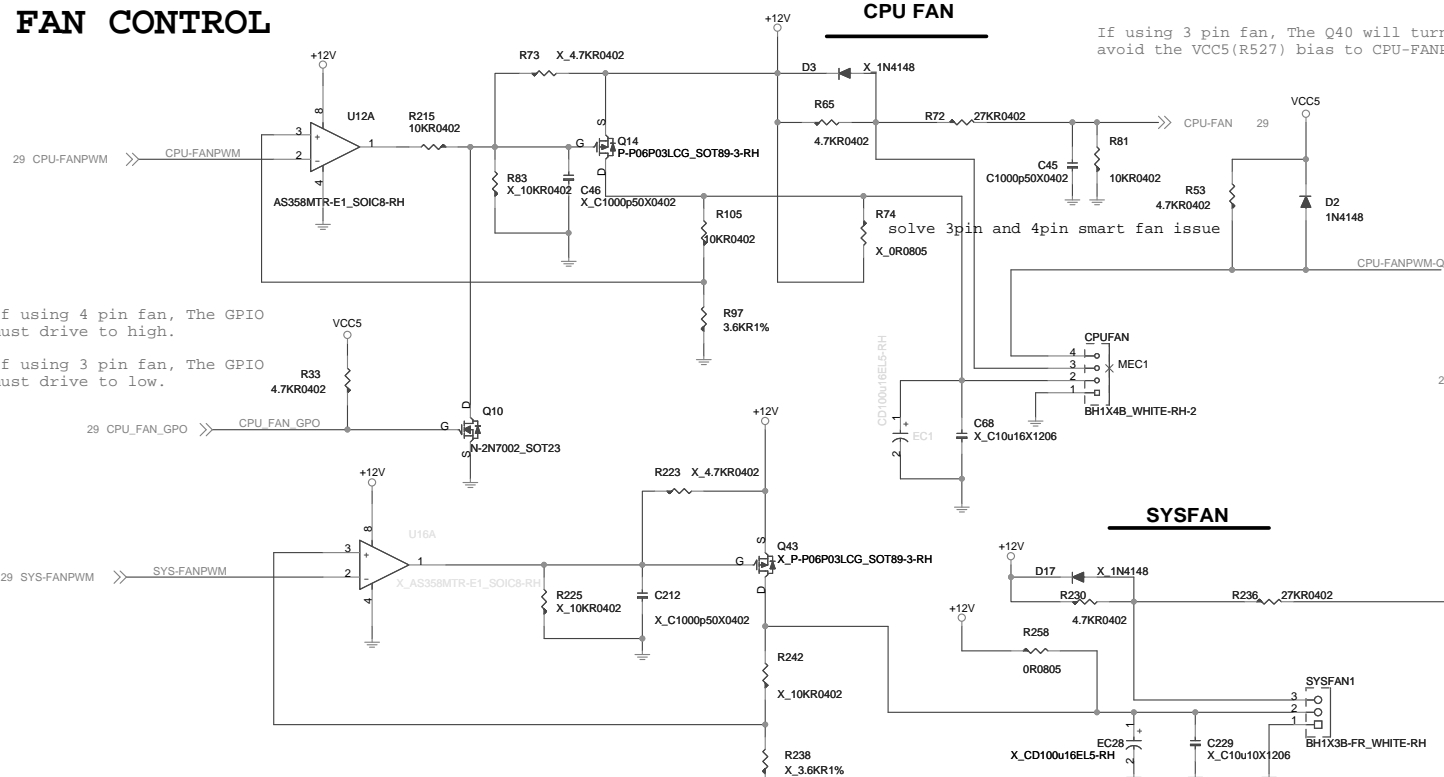
Mounting Holes



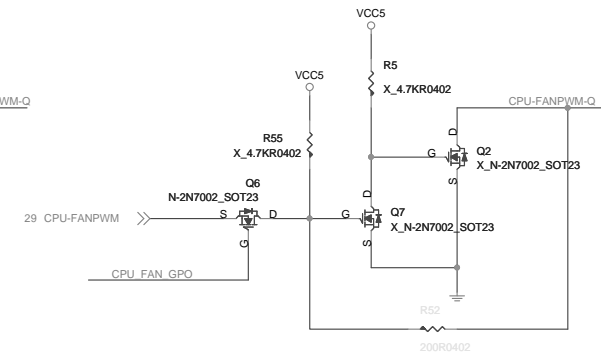
Simulation



FAN CONTROL



SYSFAN



Micro Star Restricted Secret		
Title	IDE Conn / FAN	Rev
Document Number	MS_7623	1.0
MICRO STAR INT'L CO. LTD. No. 68, Li-De St, Junde City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 29, 2009 Sheet
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To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

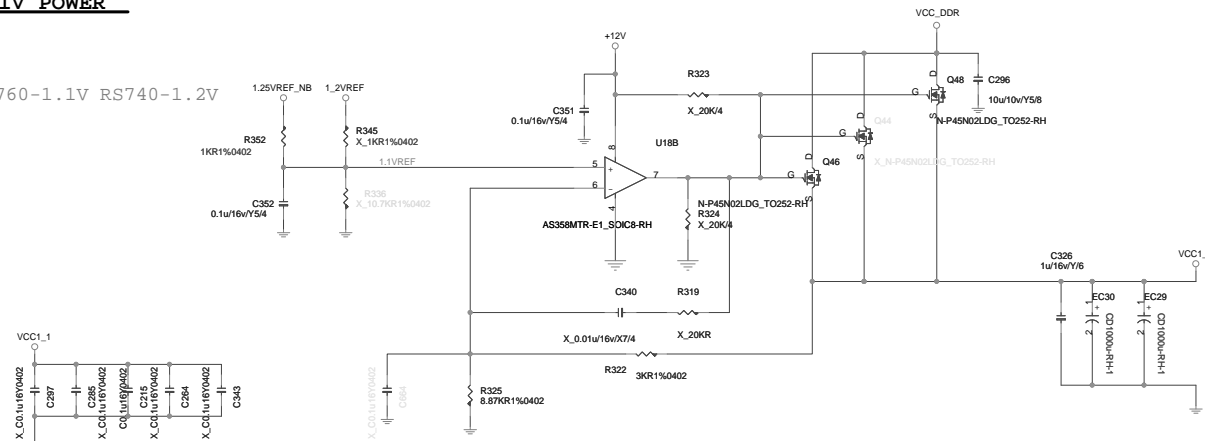
uP7711_SOP-RH

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

REF10
OPT
X_470uF/6.3V/SOLID

REF12
OPT
X_820uF/2.5V/SOLID

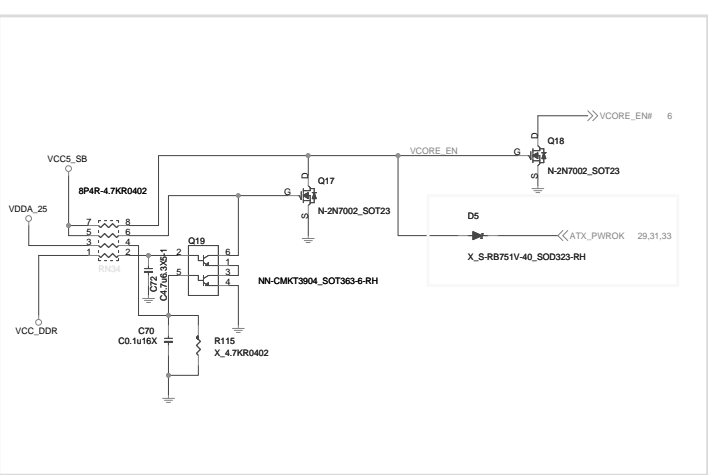
VCC1_1:RS780/RS760-1.1V RS740-1.2V

[illegible]

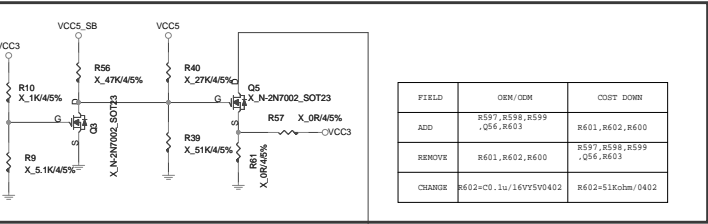
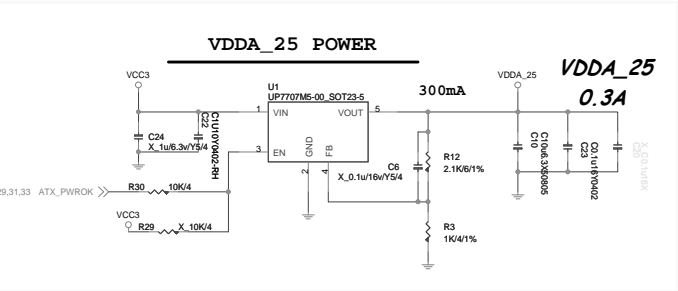
VCC_DDR:
H-MOS主料: D03-0903B4B-N03、AVL: D03-0480900-O05
L-MOS主料: D03-0603B2B-N03、AVL: D03-0480600-O05

VCC_DDR

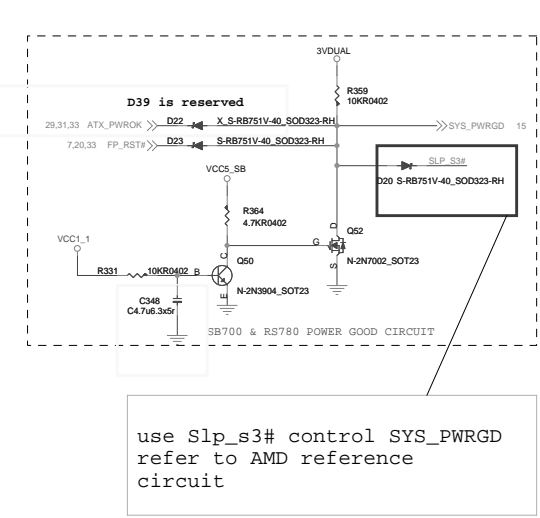
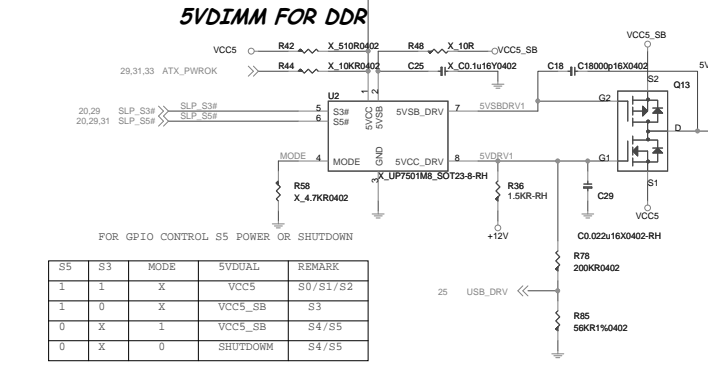
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VCC_DDR&VCC1_1 NB		1.0
Document Number		
MS_7623		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 29, 2009 Sheet 31 of 37



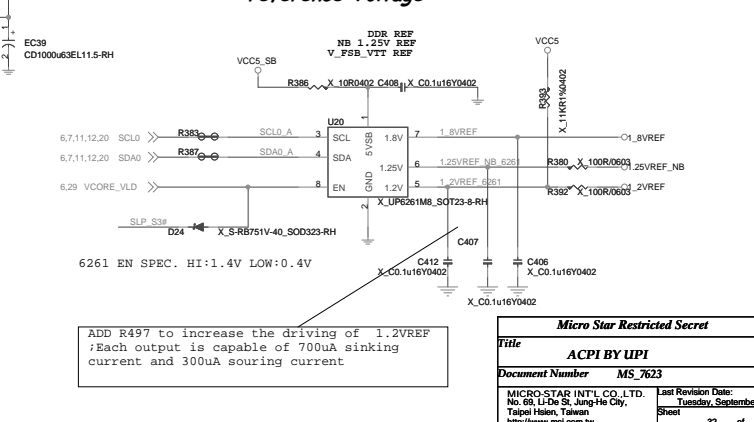
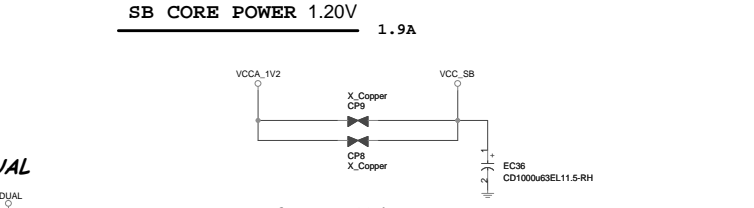
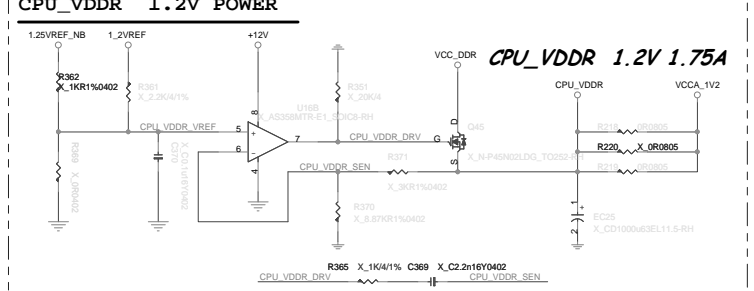
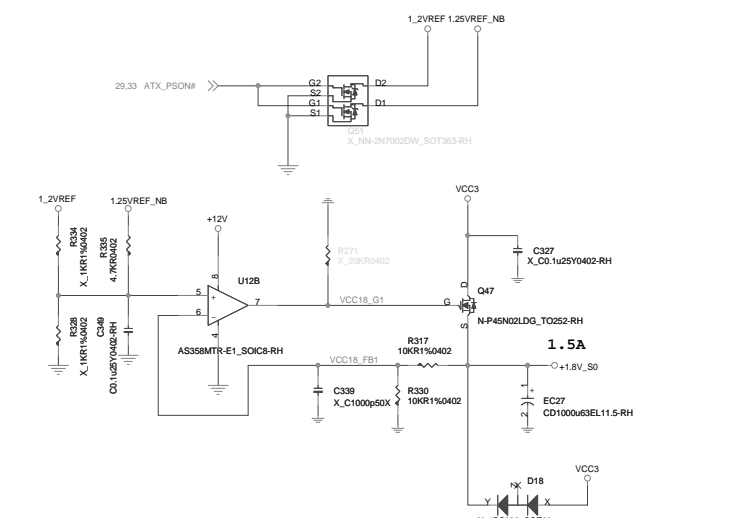
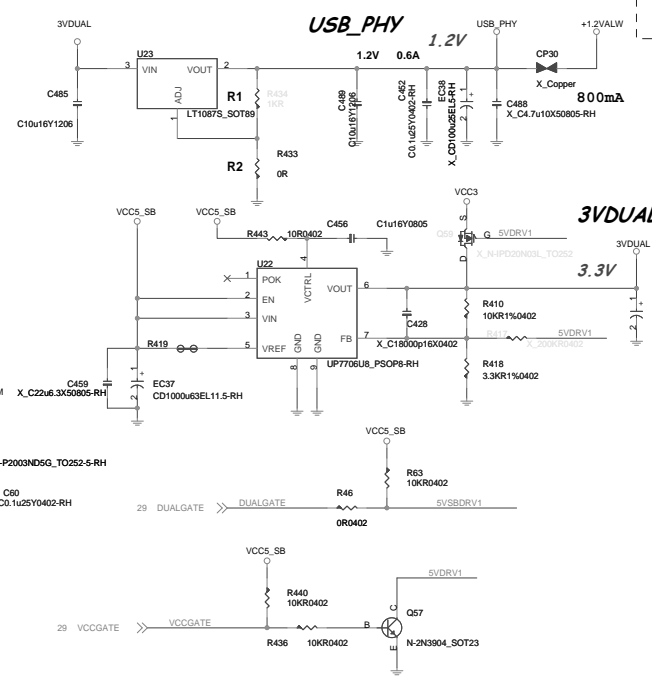
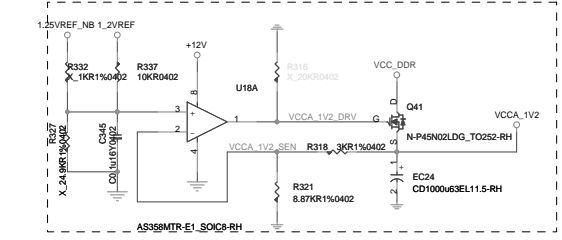
Chage 1087 to 7707 for Power up sequence



FIELD	ORIG/DEM	COST DOWN
ADD	R597,R598,R599,Q56,R603	R601,R602,R600
REMOVE	R601,R602,R600,Q56,R603	
CHANGE	R602+0.1u/16V/5402	R602+51kOhm/0402



use Slp_s3# control SYS_PWRGD refer to AMD reference circuit



ADD R497 to increase the driving of 1.2VREF
Each output is capable of 700uA sinking current and 300uA sourcing current

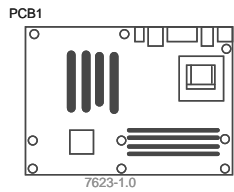
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Title	ACPI BY UPI	Rev 1.0
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Intel Front Panel

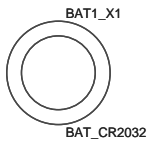


Title ATX/Front Panel/KB/EMI		Rev 1.0
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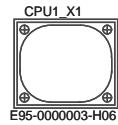
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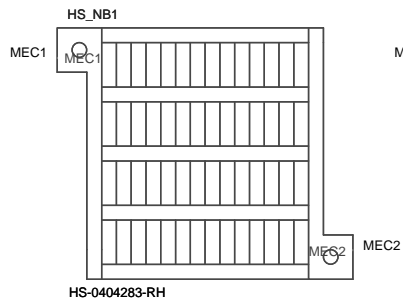
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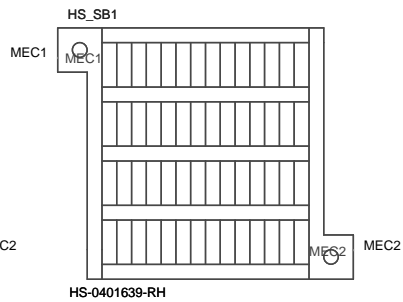
CPU RM



NB HEATSINK

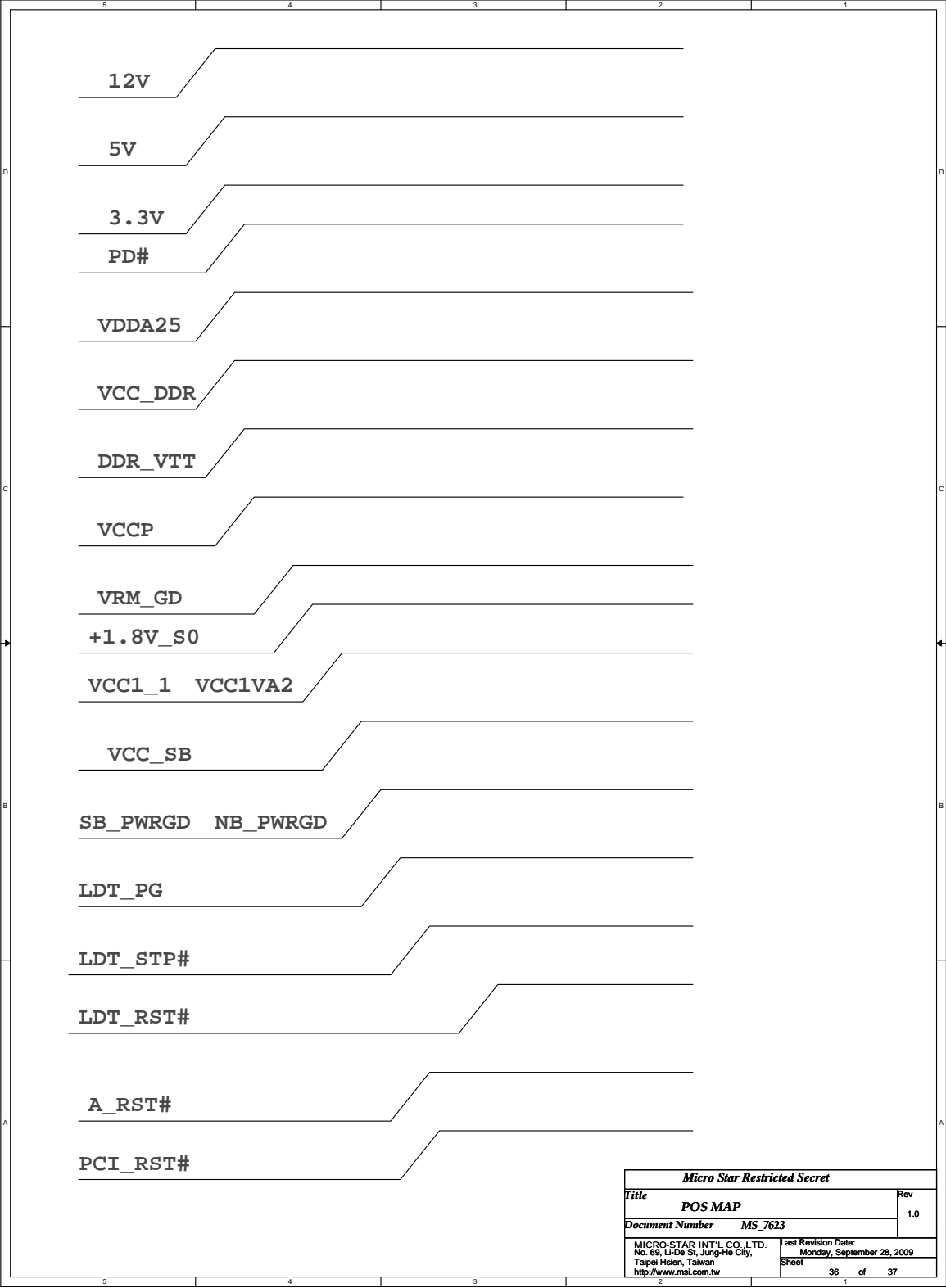


SB HEATSINK



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7302 Modify list

1:change u40 pin10:pull down to gnd
2:1.2VUSB_PHY power change to 1087

7302 1.0 Modify list

1:R309 change from 5% to 1%
2:R183,R185 will be stuffed
3:IDE_RST#,SB_PWRGD pull to 3VDUAL
4:LAN 8111C TX coupling cap change to 0.22UF
5:6261 SM BUS1 change to SM BUS0
6:JFP2 circuit update
7:CPU VDDA25 regualtor change from 1087 to 7707
8:Lan 8111c CTL_18 C285 is not stuffed
9:SB_TEST2 change to pull up to 3VDUAL
10:NB core power VCC1.1 regualtor
change to Linear Mode,including its peripheral componets
11:D39 is added for being reserved
12:C66 is added for decoupling
13:RGB PI filter changes for EMI and SI

7302 1.1 Modify list

1.Add 3 resistros for Phenom CPU in ADM AP note
2.use Slp_s3# control SYS_PWRGD refer to AMD reference circuit
3.Use ATX_PSON# to control 1.2VREF and 1.25VREF when entry S3
4.Add TAIPEI solution for coolmaster 700W issue
5.1.8Vref is controled by S3_STATE instead of SLP_S5#
6.EMI suggest to add R500

7302 1.2 Modify list

1.Change CLK GEN to RTM880N-793
2.AUDIO output CAP cost down
3.Change LAN solution to 8111DL co-lay 8103E
4.Change CPU library
5.Change VRM solution and keep the same as MS-7549 1.4
6.Delete I394 module
7.SIO change to F71889 and change LPT connector to PIN header
8.Make SB CORE power sharing the source of HT power

7623 0A Modify list

1. P19 CHANGE SATA CONNECTOR TO 90 DEGREE
2. P33 CHANGE THE FOOTPRINT OF PS2 TO ELLIPSOIDAL HOLE.
3. P8-12 CHANGE TO AM3 AND DDRIII
4. P32 ADD CPU_VDDR POWER
5. P20&P25 add one usb pin header.
6. P32/P30 Swap U48B/U50A
7. P10 change Vddr far pin to CPU_VDDR_B.
8. P27 add c236 for EMI.
9. P28 swap
CN10.1 FRONT_MIC
CN10.3 MIC_VREF
CN10.5 LINE_OUT_R
CN10.7 LINE_OUT_L
RN50.2 D22.Y
RN50.4 D22.X
RN50.6 D25.Y
RN50.8 D25.X
RN50.1 FRONT_MIC_D
RN50.3 MIC_VREF_D
RN50.5 LINE_OUT_R_D
RN50.7 LINE_OUT_L_D

9. P31 Change VCC1_1 to linear mode.
10. P31 add EC3
11. P29 reserve USB_mode pull up to 5Vdimm.
12. P29 delete D5, D7, D8.
13. P6 CHANGE LED Control Circuit.
14. P27 reserve snubber circuit for emi at net:LX
15. P28 swap RN53, RN50
16. P30 ADD FAN SOLUTION.
17. P28 SWAP R51
18. P28 USE VCC3, NOT 3VDUAL
19. P33 reserve 3 resistors between Vcc3 and GND.
20. P19 CHANGE SATA1_2 TO SATA1 AND SATA2.
21. P32 STUFF R189 3K1% AND R194 8.87K1%.
22. del JUSB3.
23. reserve C76 for EMI.
24. P15 FOLLOW CHECKLIST CHAGNE R218 TO 1KR, R221 TO 330R.
25. P15 ADD R833.
26. P20 RESERVE R492.
27. P8 ADD R834.
28. P29 CHANGE FOOTPRINT OF R311, R323 TO 0603.
29. P15 FOLLOW THE NEW CHECK LIST(SB700 1.05) NET: LDTSTOP# OF RS780L
NEED TO BE PULL HIGH TO 1.8V NOT 3.3V. SO ADD R242 FOR RS780L.
30. P15 ADD R246 FOR AMD REQUEST.
31. P29 RESERVE VREF TO VCC3.
32. P32 reserve Vref of CPU_VDDR.
33. P8 SWAP RN24.1 AND RN24.3
34. P27 Follow Athos suggestion dirctely short pin34 to gnd
35. P27 change footprint of R688 to R0603.
36. P16 DELETE C274, R259.

7623 0A cost down Modify list

1. R193, R194, R185, R209 0ohm to footprint NC_0402_6.
2. CHAGNE MODE OF LEVEL SHIFT(LDT_PWRGD TO PWROK_PWM).
3. RESERVE C664.

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